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Partner IP Core

IntelliProp

NVMe Bridge Platform

AXI-Stream Intercept NVMe Sandbox IP

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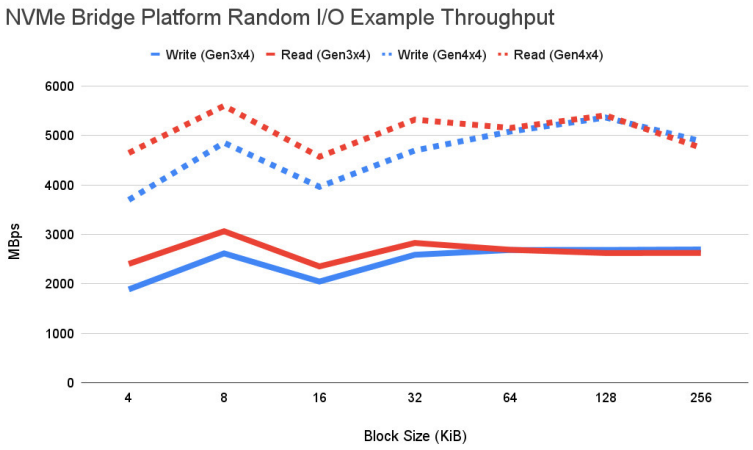
Computational storage drives (CSD) allow storage endpoints to provide computational storage functions (CSF) to offload host processing and reduce data movement. Functions such as eBPF processing, encryption, compression, filesystem management, and RAID are ideally suited for IntelliProp's NVMe Bridge Platform (NBP) IP Core.

The IntelliProp IPC-NV171B-BR NVMe Bridge Platform (NBP) uses the IntelliProp NVMe Host Accelerator Core and the IntelliProp NVMe Target Core to create an NVMe protocol bridge. The bridge is architected such that the command submissions, completion notifications and data transmissions may be either passed through without interruption or intercepted for analysis or modification. The architecture interfaces to a "Sandbox" area with an AXI Stream protocol so that IntelliProp customers can implement their own custom RTL and/or firmware in the bridge.

key features

- Customizable sandbox with **AXI-Stream interface**
- **Up to 6200 MB/s PCIe Gen4x4**
- **PCIe Switch Support** for multiple SSDs



Features

- Fully compliant to the NVM Express 1.4c industry specification
- Automated initialization with PCIe Hard Block
- PCIe switch support for multiple SSDs
- Automated command submission and completion
- Scalable I/O queue depth
- Decoupled front and back-end interfaces allows flexible user logic and applications
- Flexible data buffer type and size
- AXI Stream driven command and data paths
- Data Stream includes command parameters inline
- Support for block sizes from 512 byte to 4kB
- Application layer interface allows the processor to assume control or modify Admin commands
- Verilog and VHDL wrappers

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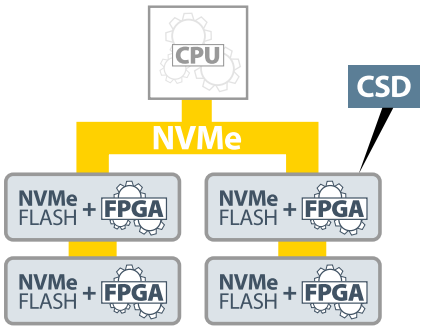
Applications

The NBP IP can be used in Computational Storage Drives (CSD) or Computational Storage Arrays (CSA) with PCIe Gen4 to Host, and multiple PCIe Gen4 SSDs through a switch or separate PCIe connections.

Functional Description

The IntelliProp NBP (IPC-NV171B-BR) implements a protocol bridge by receiving and parsing commands via the IntelliProp NVMe Target Core and forwarding them to the IntelliProp NVMe Host Accelerator Core for delivery to the NVMe SSD Endpoint. Customizable bridging logic between these two cores facilitates command management, including forwarding and tracking outstanding commands and routing data accesses appropriately, while use of the "Sandbox" area provides visibility and flexibility into the buffered data as it is transferred between the Host and the Target.

Registers in the bridging logic provide firmware with a mechanism to control data movement, to manually issue individual commands, and to control status and behavior of the bridging function. A processor or other management agent is expected to receive and properly complete administrative commands from the NVMe Target Core, while I/O commands are executed autonomously by the bridging logic. As a result, the NBP provides transparency between the Host and the Endpoint SSD, while offering the designer flexibility in command and data manipulation.



What is a Computational Storage Drive (CSD)?
A storage element that provides Computational Storage Services and persistent data storage.

Detailed Feature List

Overall

- Complete off-the-shelf solution; operational out-of-the-box
- Supports multiple NVMe SSDs (or HDD) directly or via an included PCIe Switch
- PCIe Gen4 to Host, and multiple PCIe Gen4 SSDs through a switch or separate PCIe connections
- Sandbox with AXI Stream interface for Control and Data
- System attached processor for additional flexibility in computational functions

Sandbox Specific

- Four AXI Stream interfaces provide commands, completions, and data (full duplex including sideband metadata)
- Processor connections for additional flexibility
- Implement options include RTL or FW for acceleration

FPGA/Hardware Specific

- PCIe Gen4 hard blocks pre connected
- 6200 MB/s throughput maximum (Gen4x4 interface)
- Integrated with Intel Quartus 21.3 Pro tools
- Synthesis scripts and timing constraints

NVMe Bridge Platform IP Core Facts	
Provided with core	
Documentation	Comprehensive User Documentation
Design file formats	Encrypted Verilog
Constraints files	Provided per FPGA
Verification	ModelSim verification model
Instantiation templates	Verilog (VHDL wrappers available)
Reference designs and application notes	Synthesis and place and route scripts
Additional items	Reference design
Simulation tool used	
QuestaSim (contact IntelliProp for latest versions supported)	
Support	
Phone and email support will be provided for fully licensed cores for a period of 6 months from the delivery date.	
Notes	
Other simulators are available. Please contact IntelliProp for more information.	

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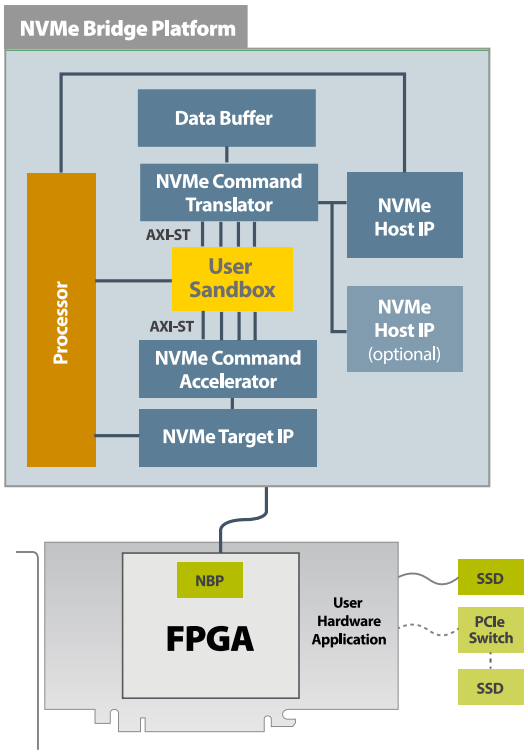
Block Descriptions

NVMe Target Core
The NVMe Target Core is the standard release IntelliProp core (IPC-NV163A-DT), and defines hardware that works in conjunction with the PCIe core to implement a compliant NVMe device interface. The NVMe Target IP core retrieves a command submission entry from the system host via the PCIe interface, and places the entry in one of many command FIFO's. Upon receipt of a command completion, the NVMe Target core automatically populates internal fields and posts the completion to the host system.

NVMe Command Accelerator
Automated internal state machines interact with the NVMe Target IP core to fetch submission queue entries and post completion queue entries. Data and commands are presented to user logic via 4 AXI Stream interfaces. There are two data AXI streams (full duplex), a command context stream and a completion context stream. Upon receipt of an IO command from the NVMe Target Core, the NVMe Command Accelerator forwards the command via an AXI Stream, then interacts with the PCIe Endpoint Core to move data between the user system and the NVMe host. Integrated registers allow user control of system configuration and core status.



NVMe Command Translator
The NVMe Command Translator negotiates NVMe commands, data, and completions with the NVMe Command Accelerator via 4 AXI stream interfaces. There are two data axi streams (full duplex), a command context stream and a completion context stream. Upon receiving a command, this block allocates buffer space to accommodate the data transfer from the NVMe SSD, then forwards the command to the NVMe Host Accelerator for issuance to the SSD. Upon return of both data and the NVMe completion from the SSD, this block returns a completion to the NVMe Command Accelerator and deallocates buffer space. Integrated registers allow user control of system configuration and core status.

Sandbox
The user logic space in the NBP allows flexibility for users to insert custom logic between the NVMe Command Accelerator and Command Translator. This logic must comply with the standardized AXI stream interfaces to transfer commands, completions, and data. Commands and completions may be either passed through directly, or modified (and tracked internally) at runtime. Data contains command parameters inline, and may therefore be dissociated from the corresponding command context. Without restrictions on data ordering or latency, user logic may take a variety of forms depending on the application.

NVMe Host Accelerator Core
The NVMe Host Accelerator core is the standard release IntelliProp core (IPC-NV164A-HI), and implements hardware to build commands in a command queue and notify the NVMe SSD of the available commands via the PCIe Root Complex core interface. The NVMe Host Accelerator core has a hardwired interface to setup commands and retrieve completions. The AXI slave and NVMe Host Accelerator core registers are also available to allow a microprocessor to setup command submissions and retrieve completions.

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Deliverables

The core includes everything required for successful implementation:

- Encrypted synthesizeable RTL code for IP core definition
- Encrypted ModelSim/QuestaSim simulation model
- Comprehensive user documentation
- Reference design
  - Example simple reference project including:
    - NVMe Host Accelerator IP core instance
    - NVMe Target IP core instance
    - NVMe Command Accelerator
    - NVMe Command Translator
    - Example Sandbox block
    - Processor
    - Memories
  - Synthesis and Place & Route scripts
  - Reference core control Firmware

Terms and Conditions

Modifications: Core modifications are generally not permitted to IntelliProp's IP cores. Any modifications that are requested must be presented to IntelliProp to determine the plausibility of integrating such changes.

Support: Phone and email support will be provided for fully licensed cores for a period of 6 months from the delivery date.

Supported FPGA Devices

Device	Speed	ALUTs	FFs	M20k
Intel Agilex F-Series	-2	31674	22136	190
Intel Stratix 10 DX	-1	31589	20038	190

Supported FPGA Cards

Manufacturer	FPGA Card
BittWare	Agilex IA-840F

To learn more, visit **www.BittWare.com**

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