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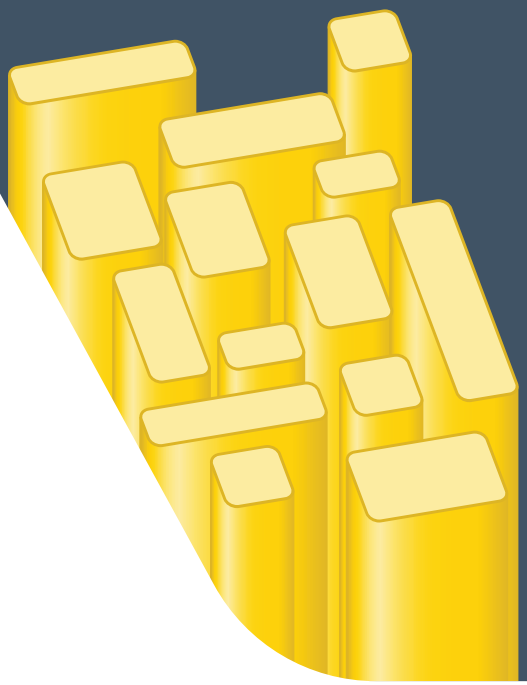
Partner Solution



GROVF
Accelerating Big Data Analytics

RDMA

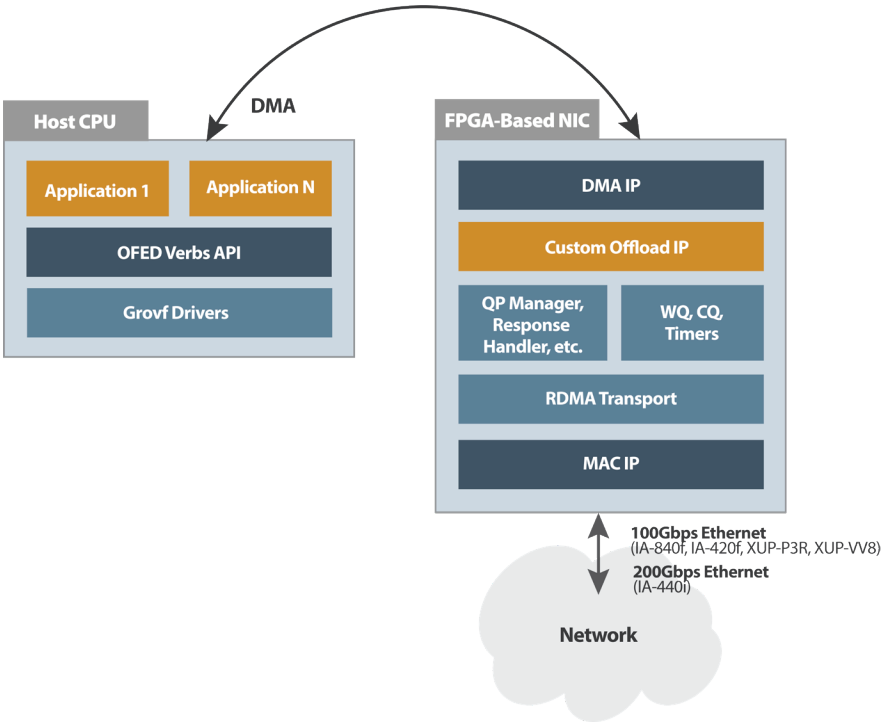
IP Core for RoCE v2 at 100/200Gbps

The GROVF RDMA IP core and host drivers provide RDMA over Converged Ethernet (RoCE v2) system implementation and integration with standard Verbs API. The RDMA IP is delivered with a reference design that includes the IP subsystem itself, the 100/200G MAC IP subsystem, the DMA subsystem, host drivers, and example application on software. The system drivers are integrated with OFED standard Verbs API and are compatible with well-known RNIC cards and software. The IP core also provides a low-latency FPGA implementation of RoCE v2 at 200Gbs or 100Gbps throughput.

Compatible with RNIC and soft RoCE v2

200Gb/s throughput, 2.7µs latency

Configurable number of RDMA queue pairs



Overview of the system architecture

Features

- Hardware operated RC, XRC, RD, UC, UD services
- Incoming and outgoing SEND, RDMA READ, RDMA WRITE
- Memory protection domains implemented in FPGA and ECN
- 3rd party MAC and DMA IPs
- Standard Verbs API on Host Machine
- Dynamic configuration using Verbs API
- Hardware retransmission and reordering
- Customizable IP

RDMA
IP Core for RoCE v2

Product Operation

The solution is a soft IP implementing RDMA over Converged Ethernet protocol. It consists of FPGA IP integrated with MAC and DMA, plus the host CPU drivers and is compatible with a variety of BittWare's FPGA cards. The 200Gbps IP is compatible with BittWare's IA-440i Agilex 7 I-Series FPGA card, and the 100Gbps IP is compatible with BittWare's IA-840f and IA-420f Agilex 7 F-series cards and XUP-VV8 and XUP-P3R UltraScale+ FPGA cards. The solution complies with Channel Adapter and RoCE v2 requirements as stated in the IB specification. The diagram on page 1 shows a simplistic architectural overview of the system. The data plane and reliable communication is hardware offloaded and the implementation does not include CPU cores in the FPGA.

Detailed Feature List

- Fully compatible with known RNIC products and soft RoCE implementations (RoCE v2)
- 100 or 200 Gb/s throughput
  - Configurable RDMA queue pairs
  - 1023 or more
- **200Gbps IP:** under 2.7 µs software to software latency (roundtrip) and under 1 µs hardware to hardware latency (roundtrip)
- **100Gbps IP:** under 2.0 µs software to software latency (roundtrip) and under 300 ns hardware to hardware latency (roundtrip)
- Hardware retransmission management
- Memory protection domains implemented in FPGA
- Congestion control using ECN, PFC
- Can work with 3rd party MAC
- Dynamic configuration using Verbs API
- Standard Verbs API on host machine user / kernel space
- Hardware implemented Reliable Connection (RC), Extended Reliable Connection (XRC), Reliable Datagram (RD), Unreliable Connection (UC), and Unreliable Datagram (UD)
- Incoming and outgoing SEND, RDMA READ, RDMA WRITE

Reference Designs

The reference example consists of three parts:

- Encrypted FPGA IPs with reference design which implement RDMA protocol
- Software drivers which provide standard Verbs API support for the FPGA-based RDMA adapter
- Example application build on top of the Verbs API demonstrating ping-pong test results: latency and bandwidth

Compatible FPGA Cards

100Gbps

- IA-840f
- IA-420f
- XUP-VV8
- XUP-P3R

200Gbps

- IA-440i

Looking for a different card? Ask us about other compatible card options.

To learn more, visit **www.BittWare.com**

v0 | last revised 2025.01.09

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