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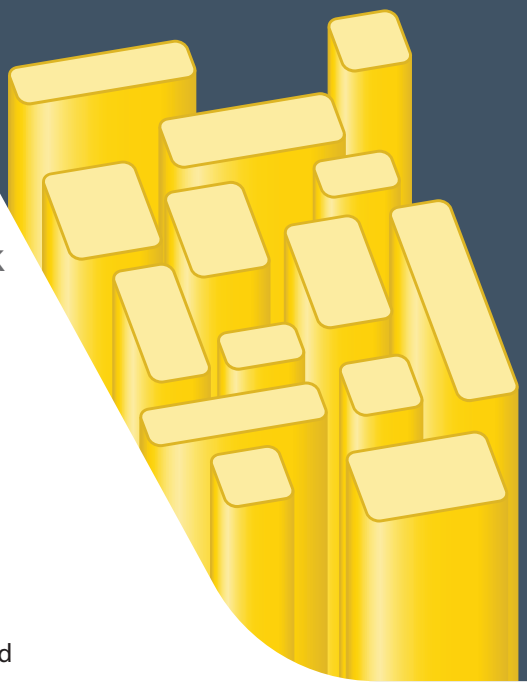
Partner Solution



exegy nxFrameWork

Low-Latency Development Framework

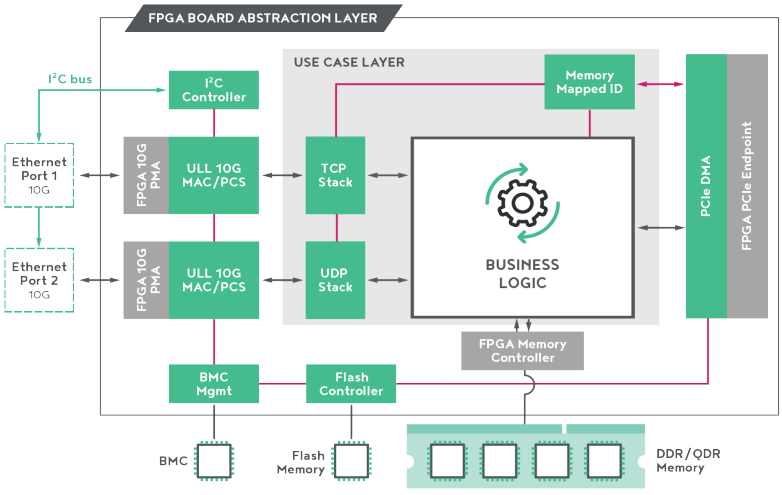
The Enyx Development Framework (nxFramework) is a hardware and software development environment designed to efficiently build and maintain ultra-low latency FPGA applications for the financial industry. Based on 10 years of research and development, nxFramework is the foundation for all Exegy off-the-shelf solutions and provides clients with the toolchain to manage a large portfolio of applications.

Developed for building in-house high-performance trading engines, order execution systems, pre-trade risk check gateways, and custom projects — any skilled FPGA developer starting a new low-latency project, maintaining an existing one, or looking to change platforms can immediately reduce their time-to-production with nxFramework.

10G MAC/PCS @ 29ns RTT

10G TCP @ 53ns RTT

Library of **60+ utility cores**



nxFramework Overview

Features

Ultra-low latency connectivity cores

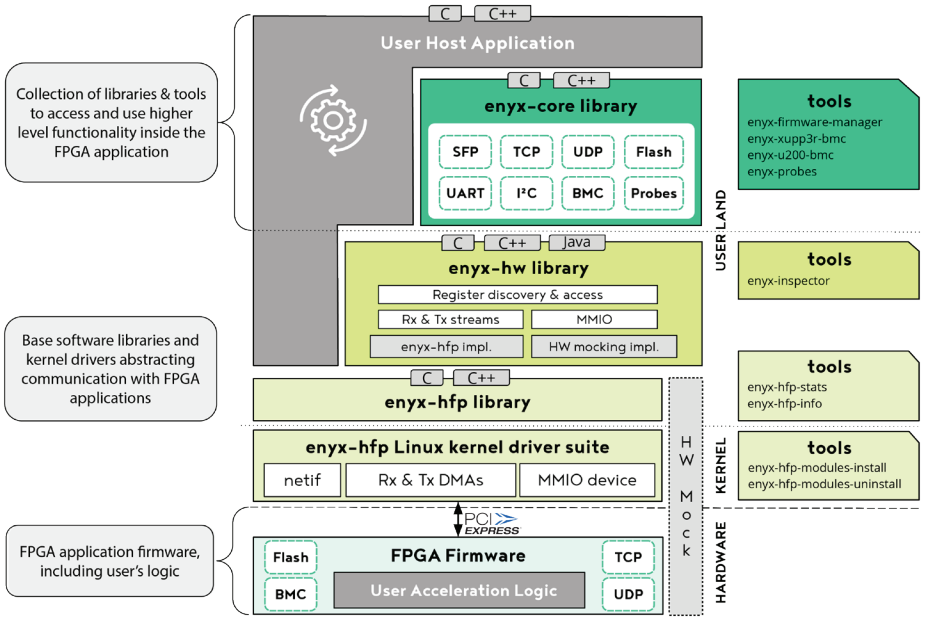
- 10G MAC/PCS - 29ns RTT - SOP to SOF @ 322MHz
- 40G MAC/PCS - 55ns RTT - SOP to SOF @ 322MHz
- 10G TCP stack - 53ns RTT @ 322MHz
- 10G UDP stack - 43ns RTT @ 322MHz
- PCIe streaming DMA - 790ns RTT @ 250MHz

Library of 60+ utility cores

- MMIO core library
- Packet streaming core library
- Memory management core library
- Math core library
- Statistics core library
- Simulation helpers library

nxFramework

Low-Latency Development Framework



Enyx Runtime Software Stack

Enyx Runtime Software Stack

Enables simple configuration and monitoring of Enyx connectivity & utility cores, including interaction with the FPGA application via our C/C++ libraries.

Hardware Development Environment

A Python scripted development environment that enables users to simplify their development cycle and accelerate their time-to-production.

The Enyx Inspector: Efficient Debugging

Equipped with a web-based GUI that can configure and monitor the FPGA at runtime, allowing for quick deployment and debug.

Detailed Feature List

- All available Enyx connectivity and utility cores
- Board management cores:
  - Flash controller support for FPGA bitstreams
  - I²C bus controller for SFP/QSFP communication
  - Configurable instantiation of memory controllers (DDR4, QDR II+)
- Additional elements included:
  - The Enyx Inspector: a web-based debugging tool
  - Linux drivers & configuration/communication libraries
  - Off-the-shelf, configurable reference designs
  - Support for widely used FPGA families in the financial sector

Compatible FPGA Cards

- XUP-P3R
- XUP-VV8

Looking for a different card? Ask us about other compatible card options

Reference Examples/Use cases

ULL Tick-to-trade platform

- Standard reference design for ULL tick-to-trade FPGA trading strategies
- nxFramework provides all the required hardware & software modules to assist with development
- Sub 100 ns RTT latency

Pre-trade Risk Check Gateway

- Standard reference design for risk checks gateway acceleration
- Two distinct TCP stacks connect respectively to the users and to the exchange
- Sub 1 µs RTT latency

To learn more, visit **www.BittWare.com**

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