

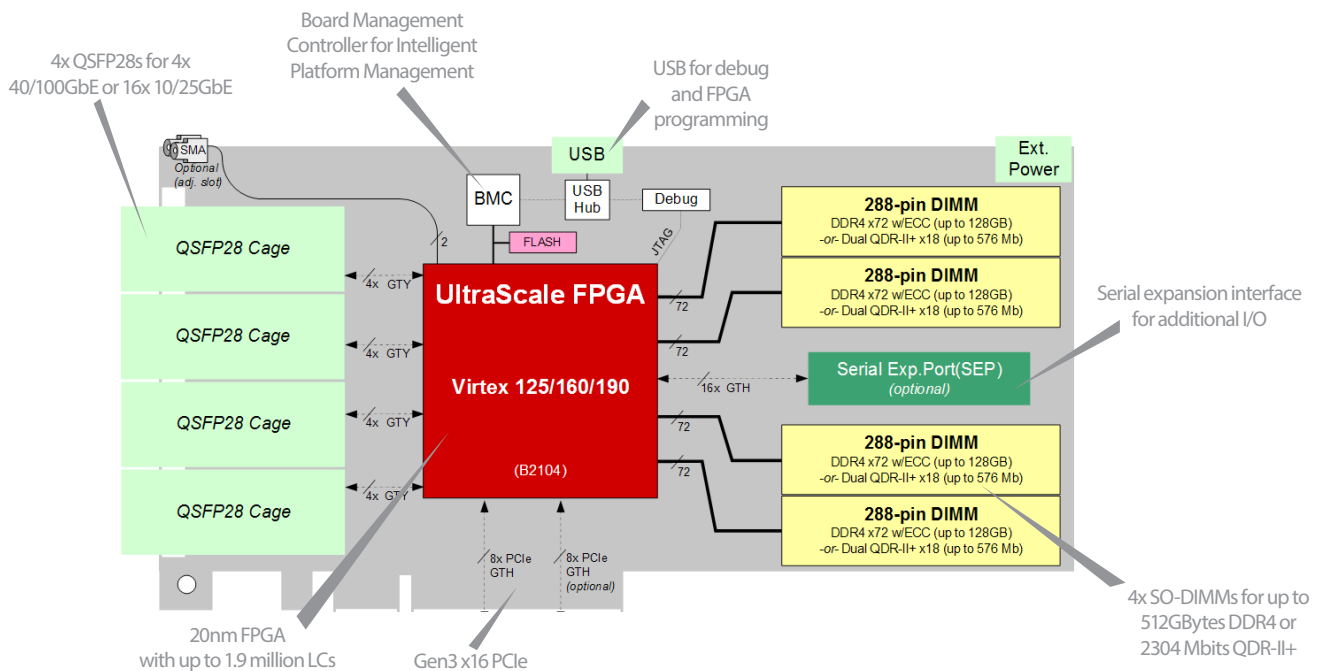
UltraScale PCIe board with up to VU190, Quad QSFP, and 512 GBytes DDR4

BittWare's XUS-P3R is a ¼-length PCIe x8 card based on the Xilinx Virtex UltraScale FPGA. The high-performance UltraScale devices provide increased system integration, reduced latency, and high bandwidth for systems demanding massive data flow and packet processing. The board offers extensive memory configurations supporting up to 512 GBytes of memory, sophisticated clocking and timing options, and four front panel QSFP cages, each supporting up to 100 Gbps (4x25) - including 100GbE.

The XUS-P3R also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform integration and management. All of these features combine to make the XUS-P3R ideal for a wide range of data center applications, including network processing and security, acceleration, storage, broadcast, and SigInt.

key features

- 4x 100GbE** via 4 QSFP28
- Up to 512 GBytes** DDR4
- Up to VU190: 1.9 million LCs** FPGA by Xilinx



Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

Additional specification options or accessory boards to meet your exact needs.



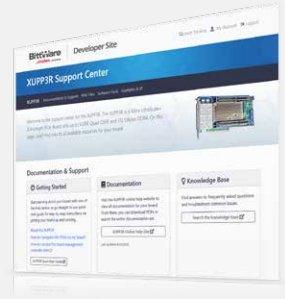
Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

| | |
|-----------------------------|---|
| FPGA | <ul style="list-style-type: none"> Virtex UltraScale FPGA <ul style="list-style-type: none"> VU190 FPGA Core speed grade - 2 Contact BittWare for additional FPGA options |
| On-board memory | <ul style="list-style-type: none"> Flash memory for booting FPGA |
| External memory | <ul style="list-style-type: none"> 4 DIMM sites, each supporting: <ul style="list-style-type: none"> Up to 128 GBytes DDR4 x72 with ECC Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks) |
| Host interface | <ul style="list-style-type: none"> Up to two 8-lane PCIe interfaces up to Gen3 (one 8x interface in a standard slot; two 8x interfaces requires a bifurcated slot) |
| Timestamping (optional) | <ul style="list-style-type: none"> 1 PPS input/output Reference clock input/output |
| USB header | <ul style="list-style-type: none"> Micro USB: (USB 2.0) for debug and programming FPGA and Flash |
| Serial expansion port (SEP) | <ul style="list-style-type: none"> Expansion interface to FPGA via 16x transceivers (optional; requires second slot) |
| QSFP cages | <ul style="list-style-type: none"> 4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 GTY transceivers Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE (100GbE, 25 GbE Virtex only) and can be combined for 400GbE Backward compatible with QSFP and can be optionally adapted for use as SFP+ |

Board Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0
- Voltage overrides

Cooling

- Standard: dual-slot active heatsink
- Optional: dual-slot passive heatsink

Electrical

- On-board power derived from 12V PCIe slot & an AUX connector (6-pin)
- Power dissipation is application dependent

Environmental

- Operating temperature 5°C to 35°C

Size

- ¾-length, standard-height PCIe dual-slot card
- 241mm x 111.15mm

Development Tools

System development

- BittWorks II Toolkit** - host, command, and debug tools for BittWare hardware

FPGA development

- FPGA Examples** - example Vivado projects
- Xilinx Tools** - Vivado® Design Suite



ALLIANCE PROGRAM
CERTIFIED

To learn more, visit www.BittWare.com

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