S5-PCIe-HQ

Intel Stratix® V GX/GS Half-Length PCIe Board with Dual QSFP+/SFP+, DDR3, and QDRII+

- High density Intel Stratix V GX/GS FPGA
- PCIe x8 interface supporting Gen1, Gen2, or Gen3
- Dual QSFP+ cages for 40GigE or 10GigE direct to the FPGA for lowest possible latency
- Up to 16 GBytes DDR3 SDRAM
- Up to 72 MBytes QDRII/II+
- Two SATA connectors
- Timestamping support
- Board Management Controller for Intelligent Platform Management
- Utility I/O includes: USB 2.0, RS-232, and JTAG

BittWare's S5-PCIe-HQ (S5PH-Q) is a half-length PCIe x8 card based on the high-bandwidth, power-efficient Intel Stratix V GX or GS FPGA. Designed for high-end applications, the Stratix V provides a high level of system integration and flexibility for I/O, routing, and processing. Over 16 GBytes of on-board memory includes DDR3 and QDRII/II+. Two front-panel QSFP+ cages allow two 40GigE interfaces (or eight 10GigE) direct to the FPGA for reduced latency, making the board ideal for high frequency trading and networking applications. The S5PH-Q also features a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform management. All of these features combine to make the S5PH-Q a versatile and efficient solution for creating and deploying high-performance FPGA computing systems.

Intel Stratix V GX/GS FPGA

The Intel Stratix V FPGA is optimized for high-performance, high-bandwidth applications with integrated transceivers supporting backplanes and optical modules. It supports 1.6 Tbps of serial switching capability and up to 3,926 18 x 18 variable precision multipliers. The Stratix V also provides PCI Express x8 via a hard IP block and supports configuration over PCI Express using the existing PCI Express link in your application. For additional flexibility, the Stratix V supports partial core reconfiguration on-the-fly while other portions of the design are running. The FPGA is supported by BittWare's FPGA Development Kit, which provides board support IP and integration.

I/O Interfaces

The S5PH-Q provides a variety of interfaces for high-speed serial I/O as well as debug support. Two QSFP+ cages are available on the front panel, each supporting 40GigE or four 10GigE channels. The QSFP+ SerDes channels are connected directly to the Stratix V FPGA, thus removing the latency of external PHYs. The QSFP+ cages can optionally be adapted for SFP+.

Two SerDes lanes are available via two SATA connectors to connect external storage devices or provide direct board-to-board communication. The x8 PCIe interface provides 8 SerDes lanes to the Stratix V FPGA. USB 2.0, RS-232, and JTAG interfaces are available for debug and programming support. The board also supports timestamping with provision for a 1 PPS and reference clock input as well as RS-232 for connection to GPS or other time sources.

Memory

Several on-board memory banks are available to the Stratix V FPGA. Memory includes up to 16 GBytes of DDR3 SDRAM (two 64-bit banks) and up to 72 MBytes QDRII/II+ (four 18-bit banks). The S5PH-Q also provides flash memory for storing multiple FPGA images.

BittWare is a preferred board supplier for Intel OpenCL, and Intel has certified the S5PH-Q to support the OpenCL SDK.

OpenCL

Board Management Controller

BittWare's S5 boards feature an advanced system monitoring subsystem, similar to those typically found on today's server platforms. At the heart of the board's monitoring system lies a Board Management Controller (BMC), which accepts Intelligent Platform Management Interface (IPMI) messaging protocol commands. The BMC provides a wealth of features, including control of power and resets, monitoring of board sensors, FPGA boot loader, voltage overrides, configuration of programmable clocks, access to I^2C bus components, field upgrades, and IPMI messaging. Access to the BMC is via PCIe, USB, or serial port. BittWare's BittWorks II Toolkit also provides utilities and libraries for communicating with the BMC components at a higher, more abstract level, allowing developers to remotely monitor the health of the board.

Development Tools

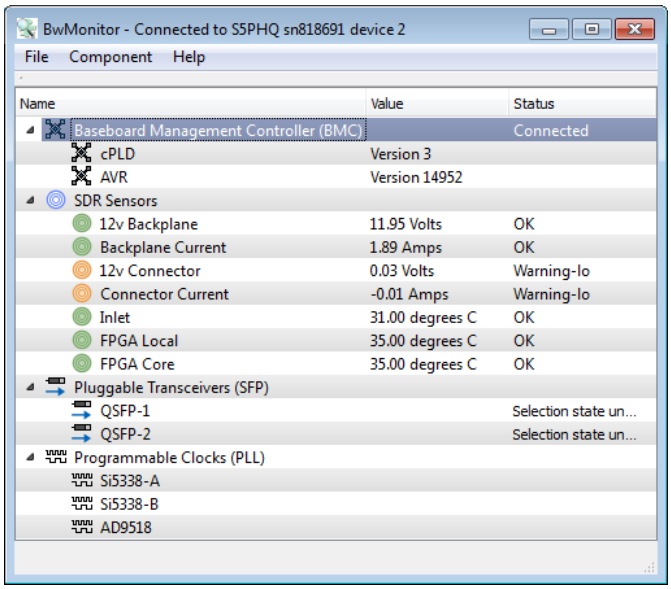
BittWorks II Toolkit

BittWare offers complete software support for the S5PH-Q with its BittWorks II software tools. Designed to make developing and debugging applications for BittWare's boards easy and efficient, the Toolkit is a collection of libraries and applications that provides the glue between the host application and the hardware. A variety of features allow developers to take full advantage of the Stratix V FPGA capabilities on the BittWare board, including FPGA control via PCIe, Flash programming, custom ISR scripts, and convenient control of FPGA loads. The Toolkit supports 32-bit, and 64-bit Windows and Linux platforms and can connect to the board via PCIe, Ethernet, or USB, providing a common API no matter the connection method.

FPGA Development Kit

BittWare's FPGA Development Kit (FDK) provides FPGA board support IP and integration for BittWare's Intel FPGA-based COTS boards. The FDK includes FPGA components that provide preconfigured physical interfaces, infrastructure, and examples, drastically cutting development time and easily integrating into existing FPGA development environments.

Working example projects are available for each board which illustrate how to move data between the board's different interfaces. Supported interfaces include DDR3, DDR2, QDR2/+, PCIe, 10GigE, LVDS, SerDes, and Double Data Rate I/O. All example projects are available on BittWare's Developer Site.



BwMonitor in the BittWorks II Toolkit provides a view into the board management capabilities of your BittWare hardware.

BittWare Firmware and Financial Solutions Partners

BittWare offers firmware for the Stratix V FPGA on the S5 family PCIe boards, targeted specifically for high frequency trading applications. BittWare's FPGA Development Kit provides a solid base for your financial application, including the following:

- 10GigE MAC
- PCIe multi-channel DMA engines
- DDR3 SDRAM and QDRII/II+ controllers

BittWare has also partnered with several companies to offer solutions for financial acceleration:

- Algo-Logic: Market feed handler and low latency gateway libraries
- Argon Design: Design services specializing in multimedia and FPGA-based high performance trading
- Atomic Rules: Custom IP development, example UDP, precision timestamping, PCIe, networking
- Enyx: UOE, TOE, book building IP, order management IP, Market Feed Handler
- InDeLabs: Market Data Feed Handler and custom services
- Intilop: Ultra low latency TOE, UOE, and MAC
- LeWiz: Ultra low latency, multi-session TOE IP cores
- PolyBus: Infiniband link layer and transport layer
- Tamba Networks: Ultra low latency Ethernet and Interlaken cores

S5PH-Q Specifications

Board Specifications

FPGA

- Intel® Stratix® V GX/GS FPGA
- 20 full-duplex, high-performance, multi-gigabit SerDes transceivers @ up to 14.1 GHz
- Up to 952,000 logic elements (LEs) available
- Up to 62 Mb of embedded memory
- 1.4 Gbps LVDS performance
- Up to 3,926 18x18 variable-precision multipliers
- Embedded HardCopy Blocks

Memory

- Two banks of up to 8 GBytes DDR3 SDRAM (x64)
- Four banks of up to 18 MBytes QDRII+ (x18)
- 128 MBytes of Flash memory for booting FPGA

PCIe Interface

- x8 Gen1, Gen2, Gen3 direct to FPGA

USB Header

- USB 2.0 interface for debug and programming FPGA and Flash

Timestamp Header

- 1 PPS input
- Reference clock input
- RS-232

Debug Utility Header

- RS-232 port to Stratix V
- JTAG debug interface to Stratix V

QSFP+ Cages

- 2 QSFP+ cages on front panel connected directly to FPGA via 8 SerDes (no external PHY)
- Each supports 40 GigE or four 10 GigE interfaces
- Can be optionally adapted for use as SFP+

Serial ATA

- 2 SATA connectors, connected to FPGA

Board Management Controller

- Voltage, current, temperature monitoring
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0 and JTAG access
- Voltage overrides

Size

- Half-length, standard-height PCIe slot card
- 168mm x 111.15mm
- Max. component height: 14.47mm

Development Tools

System Development

- BittWorks II Toolkit - host, command, and debug tools for BittWare hardware; source code porting kit also available

FPGA Development Kit

- Physical interface components
- Board, I/O, and timing constraints
- Example Quartus projects
- Software components and drivers

FPGA Development

- Intel Quartus® II software

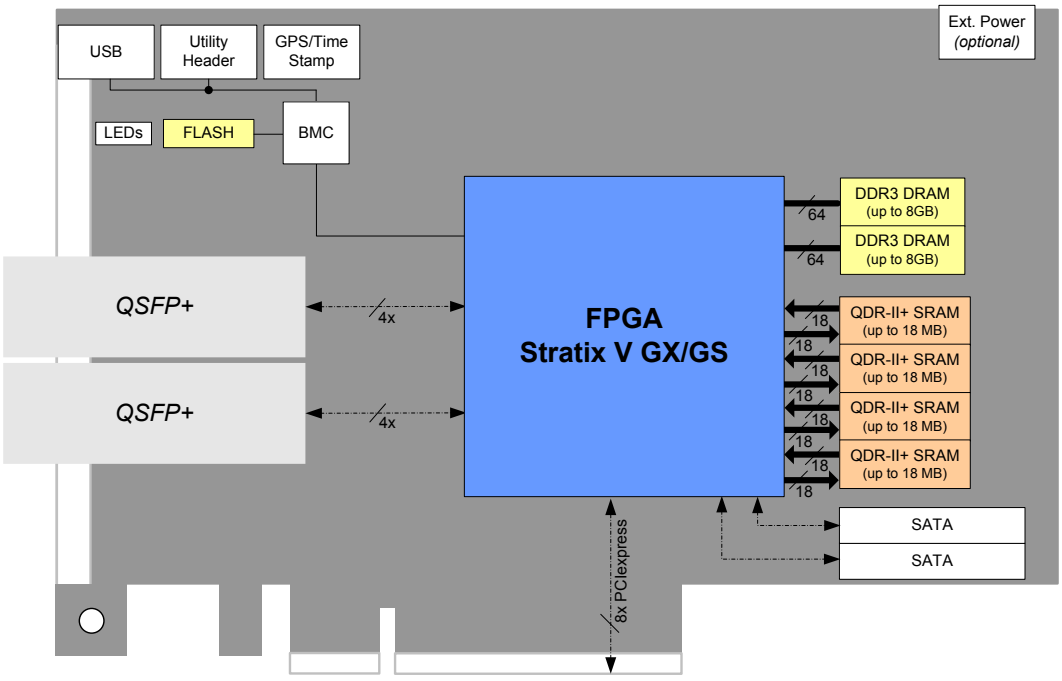
OpenCL Development

- OpenCL Developer's Bundle - BittWorks II Toolkit, Board Support Packages, Intel SDK for OpenCL, Intel Quartus II

Accessory Boards

- BittWare BWBO breakout board for JTAG and RS-232 access

Figure 2: S5PH-Q System Block Diagram



S5PH-Q Ordering Options

S5PHQ-RW-AAAAABCC-DEFGHIJKLM-O-OOQRS

RW	**Ruggedization** 0U = Commercial (0C to 50C)*
AAAAA	**Stratix V Family, HardIP, and Size** GXEA3 = Stratix V GXEA3 GXEA4 = Stratix V GXEA4 GXEA5 = Stratix V GXEA5 GXEA7 = Stratix V GXEA7* GXEA9 = Stratix V GXEA9† GXEAB = Stratix V GXEAB† GSMD4 = Stratix V GSMD4 GSMD5 = Stratix V GSMD5 GSED6 = Stratix V GSED6† GSED8 = Stratix V GSED8†
B	**Stratix V GXB Speed** 1 = 14.1 Gbps 2 = 12.5 Gbps*‡ 3 = 8.5 Gbps
CC	**Stratix V Temp/Speed** C1= Commercial Temperature Range, Speed Grade 1 C2= Commercial Temperature Range, Speed Grade 2* C3= Commercial Temperature Range, Speed Grade 3
D	**DDR3 Bank A** 0 = None A = 2GB B = 4GB* C = 8GB
E	**DDR3 Bank B** 0 = None A = 2GB B = 4GB* C = 8GB
F	**QDR II Bank A** 0 = None 2 = 9MB 3 = 18MB*
G	**QDR II Bank A Type & Speed** 0 = None 3 = QDR2 333MHz D = QDR2+ 550MHz*
H	**QDR II Bank B** 0 = None 2 = 9MB 3 = 18MB*
I	**QDR II Bank B Type & Speed** 0 = None 3 = QDR2 333MHz D = QDR2+ 550MHz*
J	**QDR II Bank C** 0 = None 2 = 9MB 3 = 18MB*
K	**QDR II Bank C Type & Speed** 0 = None 3 = QDR2 333MHz D = QDR2+ 550MHz*
L	**QDR II Bank D** 0 = None 2 = 9MB 3 = 18MB*
M	**QDR II Bank D Type & Speed** 0 = None 3 = QDR2 333MHz D = QDR2+ 550MHz*
O	**Oscillator** S = Standard*
Q	**Heatsink** A = Board Fansink Single Slot B = FPGA Fansink* C = FPGA Fansink Dual Slot D = FPGA Heatsink Dual Slot E = FPGA Heat sink single slot
R	**Misc. Configuration** 0 = Standard
S	**Environmental Assembly** 6 = RoHS 6/6* P = SnPb assembly

*Default
† Contact BittWare for availability.
‡ On GXEAB devices, the Stratix V GXB speed is 11.2 Gbps.

DS-S5PH-Q | Rev 2018.11.15 | November 2018

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