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Partner IP

Corundum

Open-Source 100G NIC IP Core

Jump-start your SmartNIC project with the open-source Corundum IP core! It's got the basic framework for FPGA-based network acceleration, ready for you to adapt and extend. The expectation is for users to add their own custom logic and host software to build SmartNICs, saving time by using the foundational network packet processing elements in Corundum. A user application area allows for easier targeting of multiple card types.

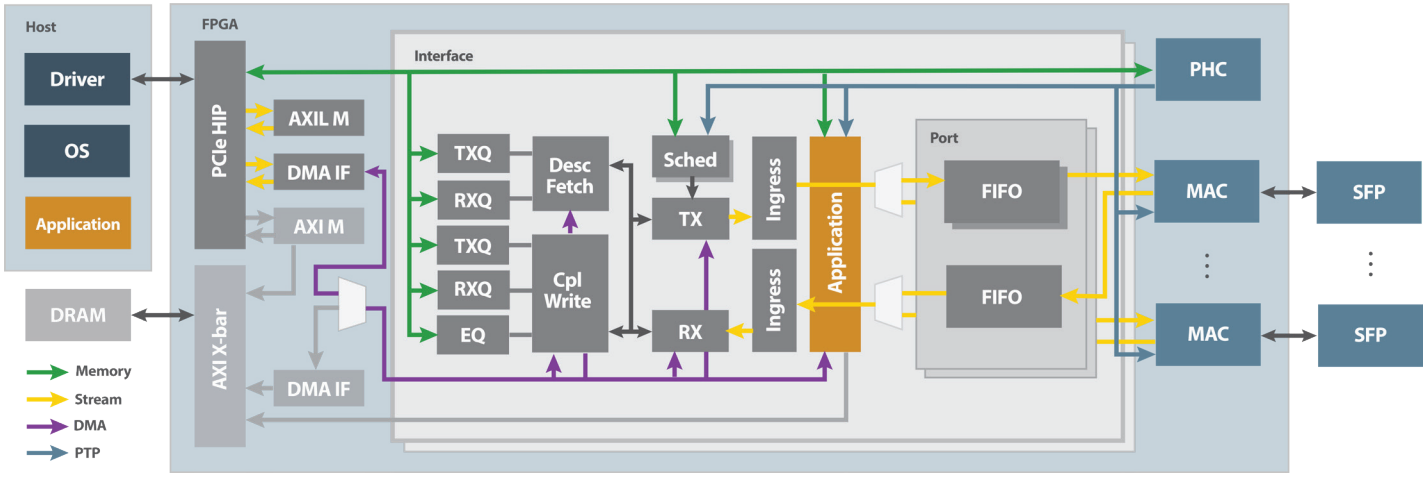
What sets Corundum apart from other open-source FPGA NIC frameworks are features like scatter/gather, PTP, and robust host DMA integration. The overall performance targets general-purpose packet processing applications at line rates up to 100 Gb/s.

The IP core targets BittWare FPGA cards with AMD (formerly Xilinx) Virtex UltraScale+ and Intel Agilex 7 devices. Specific supported cards are listed under specifications. As an open-source project, customers may use the IP to port to other BittWare cards.

Open Source for Commercial Projects

Fine-Grained Traffic Control

Designed for Customization



Features

- **Open-source FPGA-based NIC**
  - PCIe Gen3 x16, multiple 10G/25G/100G Ethernet ports
  - Fully custom DMA engine; Linux driver
- **Fine-grained traffic control**
  - 10,000+ hardware queues, customizable schedulers
- **Application block for custom logic**
  - Access to network traffic, DMA engine, on-card RAM, PTP time
- **PTP timestamping and time synchronization**
- **Management features (FW update, etc.)**

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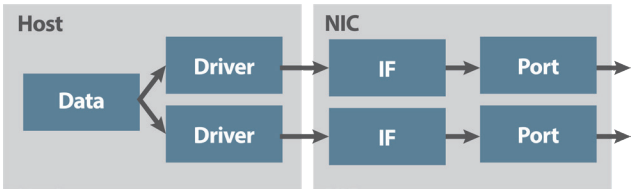
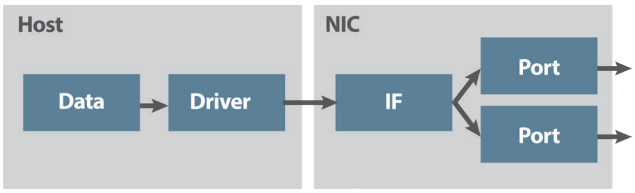
Detailed Feature List

Fine Grained Traffic Control
- 10,000+ transmit queues
  - Each queue is an independent channel between SW and HW
  - Classify in SW, control in HW
  - Fine-grained, per-flow or per-destination control
  - 128 bits/queue -> 4096 queues in 2 URAM on US+
- Transmit scheduler
  - Determines which queue to transmit from
  - Default scheduler is round robin
  - Can be used to implement traffic shaping, rate limiting, etc.

Ports and Interfaces
- Hardware support for multiple uplinks
- Multiple physical ports appear as single OS-level interface
- Ports have separate schedulers
- Migrate or stripe flows across ports by changing scheduler settings

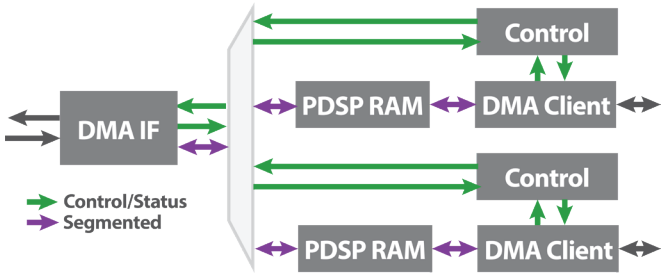


Traditional NIC: Assignment in Software



Corundum NIC: Assignment in Hardware

Modular DMA Engine
- DMA engine split between interface and client modules
  - Interface connects to host – PCIe, AXI, etc.
  - Client modules form internal ports – AXI stream, memory-mapped AXI
- Clients connected to interface with dual port RAMs
- Support both servers (PCIe) and SoCs (AXI) with same core logic



Open Source
- Corundum core logic 100% open-source Verilog
  - Including 10G/25G MACs, PCIe DMA, AXI, AXI stream, etc.
  - Device hard IP used for interfacing – PCIe, 100G MAC, serdes
- Simulation uses open-source tools
  - Cocotb + Icarus Verilog/Verilator
  - Cocotb extensions for AXI, Ethernet, and PCIe
- Tox + pytest for CI
- Makefiles for build automation

Applications
- Offload application-specific processing
- Datapath for novel transmit schedulers
- Instrument Corundum for performance measurements
- Direct transceiver access permits physical-layer measurements and development of new wire protocols
- Use core logic as a packet DMA engine in a larger system

Compatible FPGA Cards
- 250-SoC
- XUP-P3R
- IA-420f (planned for early 2023)

Looking for a different card? Ask us about other compatible card options

To learn more, visit **www.BittWare.com**

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