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Partner IP

CHEVIN TECHNOLOGY

TCP/IP Offload

Ethernet IP Core

The TCP/IP (Transmission Control Protocol/ Internet Protocol) is an Ethernet IP core for FPGAs that incorporates both the transport and internet layer protocols to deliver reliable, end-to-end network communications on the internet or private networks.

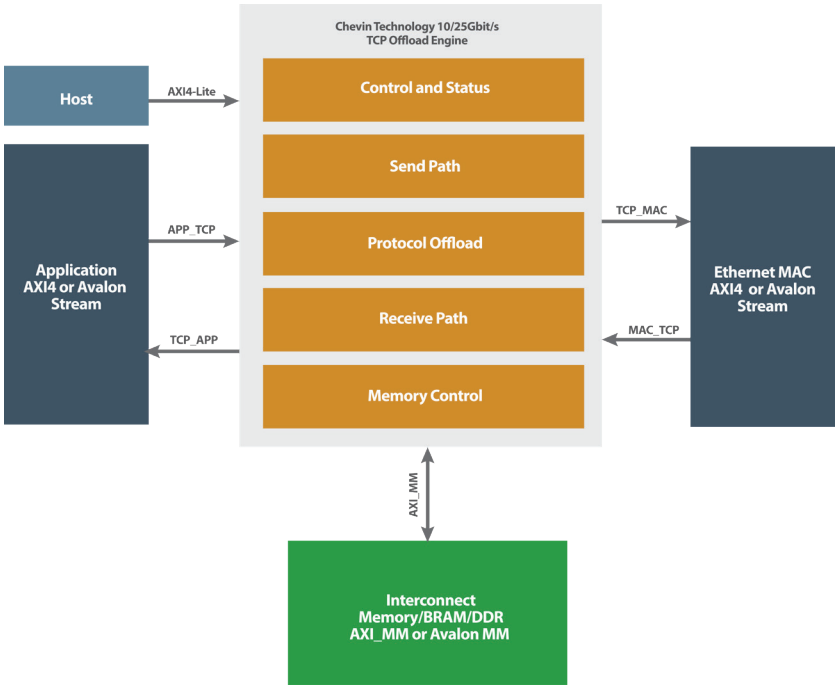
Chevin Technology's TCP/IP Offload Engine is an FPGA Synthesizable Ethernet TCP/ IP server/client in a lean and fast, all-RTL solution. The TCP IP core can be used with both 10G and 25G Ethernet IP cores for reliable, high performance connectivity in any FPGA using a minimum of resources. Chevin Technology's TCP/ IP core offloads the TCP protocol using fast and efficient logic for checksum calculation, and is easily integrated alongside other protocols to provide an easy path for the development of TCP-enabled FPGA applications.

The IP core targets BittWare FPGA cards with AMD (formerly Xilinx) Virtex UltraScale+ and Intel Agilex 7 devices. Specific supported cards are listed under specifications.

Up to 256 TCP/IP sessions

Low latency and high throughput

Up to 1GB Rx and Tx buffer



Features

- Low gate count
- 1 to 256 simultaneous TCP/IP sessions
- Server/client, configurable per session
- Low latency, high throughput performance
- Zero Copy—dynamic stream/ memory source and destination switching
- Programmable per session receive/ congestion window
- Internal/external memory
- AXI4_MM memory
- Configurable Tx and Rx buffer size: 1KB-1GB
- 64-bit AXI4/Avalon stream @ 156.25 MHz
- AXI4 MAC interface connects to any Ethernet MAC, including Xilinx, Intel and Chevin
- AXI4 routing capability on all interfaces per session - for flexible routing options to multiple applications, MACs or other interfaces

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FPGA Integration

The TCP/IP Offoad Engine provides a quick path to creating TCP enabled applications with a minimum of additional resources for network management at the FPGA side. The AXI4-Lite host interface permits control and configuration of the TCP IP core's registers and statistics for connection and link monitoring. The User application side and MAC connect to the TCP IP core with an easy to use AXI4-Stream or Avalon interface.

The TCP IP core can be configured to initiate (client) or accept (server) a TCP connection with a remote endpoint. Once a session is established, data can be reliably sent and received over the TCP protocol; taking care of checksum insertion/checking, sockets and flow control at high, sustained data rates of 10 or 25 Gbit/s. The user interface provides flow control, and manages multiple connections.

Multiple simultaneous connections are supported, limited only by available packet buffer resources. Opening and closing connections is handled by the TCP core, with no requirement for additional software support. Re-transmit is handled by a control layer within the TCP for fast, easy error recovery. Statistics are collected for all sent and received frames for traffic and connection analysis.

Specifications

Throughput and Latency Figures

CP send/receive rate: 9.5 Gbps (1.2 GB/s);
TX / RX– Latency < 1 us

FPGA Resource Figures

Device	Sessions	Resource Usage
Intel Agilex F-Series	32	IA-840F card with all features enabled including memory mapped interface: 40k ALMs, 220 M20K
Xilinx Virtex UltraScale, Zynq	16	Small memory footprint: 110 BRAMs + packet buffer; 35000 LUTs

Deliverables

- Encrypted compiled netlist
- Datasheet and User Guide
- Reference designs/examples
- Simulation Test bench
- Build scripts for Vivado, Quartus
- Software driver
- Support for integration into FPGA

Applications

- Artificial Intelligence
- Machine Learning
- Video Imaging
- Image/Signal Processing
- Internet Security Monitoring
- Data Storage & Capture Systems
- Trade Execution & monitoring
- HPC/ Big Data systems
- Data Mining

Compatible FPGA Cards

- IA-840F
- IA-420F
- XUP-VV8

Looking for a different card? Ask us about other compatible card options

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