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Partner IP Core

Atomic Rules

TimeServo
IP Core

High-Performance FPGA System Timer IP

The TimeServo IP core by Atomic Rules is an RTL IP core that serves the function of an FPGA's system timer or clock. Although specifically designed to support the needs of line-rate independent packet timestamping, TimeServo may find use where there is the need for a high-resolution, modest-accuracy timebase. TimeServo and TimeServoPTP both use a digital phase locked loop (DPLL) to control the frequency of a Numerically Controlled Oscillator (NCO). A stable reference clock (whose absolute accuracy is not important) provides the clock for the NCO.

In conjunction with a timestamp-capable MAC (not included), TimeServo can be ordered as TimeServoPTP: a complete IEEE-1588v2/PTP ordinary slave device. TimeServoPTP does not require any host processor interaction to function.

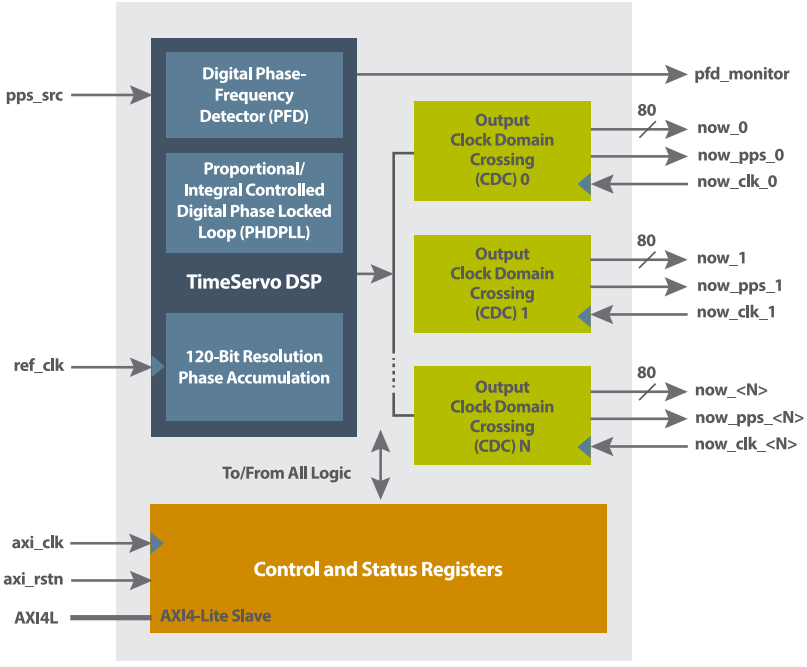
Sub-nanosecond resolution, sub-microsecond accurate FPGA system timer component

key features

1588v2 PTP Ordinary Clock

Up to **32 outputs**

1-Step + 2-Step Synchronization



Features

- Single-component solution for providing coherent time within an FPGA
- Operates with or without an externally provided Pulse-Per-Second (PPS) Reference
- Flexible and independent clocks for control-plane and reference clock
- Up to 32 outputs, each in their own clock domain
- Outputs individually runtime switchable between three 80-bit formats
  - Binary 48.32
  - IEEE Ordinary
  - IEEE Transparent
- Software control and observability from AXI control plane
- Internal logical 120-bit resolution phase accumulator
- Proportional/Integral controlled Digital Phase Locked Loop (PI-DPLL)
- Observable output of digital Phase-Frequency Detector (PFD Monitor)

TimeServo
IP Core

Operation and Clock Limits

All operation of the TimeServo is controlled though an AXI4-Lite Memory Mapped control-plane interface. A set of defined registers controls the module and returns the status. The control and status registers are always functioning when the control plane is operational.

In all cases, time is "made" from a Reference Clock signal. This reference clock should be chosen to be of the best possible stability. Its absolute frequency is less important when the digital PLL is engaged. The reference clock increments a 120-bit phase accumulator on each edge. Logic in the TimeServo DSP section statically or dynamically adjusts the fractional increment value added at each reference clock.

In the absence of an externally supplied Pulse-Per-Second (PPS) signal; TimeServo can be set, trimmed, and nudged under software control.

In the presence of an externally supplied PPS signal, the time can be set and nudged; but the frequency trim (e.g. faster/slower) is self-controlled and updated by TimeServo.

Supporting the trend of contemporary MACs having timestamp logic separated into multiple clock domains; each of the TimeServo's outputs may each be placed in their own clock domain; and up to 32 outputs may be generated by the component when instantiated.the advantages of FPGA hardware acceleration.

Reference Examples

- Software control utility to set/get common settings as well as observe behavior.
- Example design using Arkville IP Core (Arkville available separately) showing application with IEEE-1588 Precision Time Protocol (PTP).

Clock Frequency Limits (MHz)

Clock	Minimum (MHz)	Nominal (MHz)[1]	Maximum (MHz)[2]
axi_clk	50	125	500
ref_clk	100	250	500
now_clk	50	312.5	500

1 Performance Measurements made at nominal frequency
2 FPGA performance limits may prevent operation at Maximum frequency (e.g. Timing Closure)

Compatible FPGA Cards

The TimeServo IP is compatible with all current BittWare cards with Xilinx UltraScale+, Intel Stratix 10 and Intel Agilex FPGAs.

Specifications

TimeServo

- Standard AXI4-Lite Control Plane Interface
- Up to 32 80-bit time outputs, runtime switchable binary and IEEE ordinary/transparent
- Internal logical 120-bit Reference Clock Phase Accumulator
- Proportional/Integral controlled Digital Phase Locked Loop (PI-DPLL)
- Nominal Settling time: 150 s (may be changed under software control)
- Best-Case Simulated Jitter Observation +/- 2.5 ns (with 400 MHz Reference Clock)
- Nominal Real-World Jitter Observation +/- 10 ns (with 400 MHz Reference Clock)

TimeServo PTP

TimeServo PTP has all of the TimeServo features listed above plus the following:

- An IEEE 1588v2 PTP Compliant Ordinary Clock (OC) Slave Implementation for FPGA
- Supports both 1-Step and 2-Step synchronization with an external network time grandmaster
  - TimeServoPTP Delay Requests are 1-Step using MAC TX Hardware Time Insertion
- End to End (E2E) Delay Mechanism
- Single-component solution for providing coherent time within an FPGA
- Communicates with PTP Master via Ethernet L2 PTP/1588 EtherType frames
- Flexible and independent clocks for control-plane and reference clock
- Up to 32 time "now" outputs with Clock Domain Crossing (CDC) Logic
  - Each in their own Clock Domain from user-supplied clock
  - Each individually selectable 80b output format (Binary, IEEE Ordinary, IEEE Transparent)
  - Each with a Pulse Per Second (PPS) output pulse in output clock domain
- Software control and observability from AXI control plane
- Following Initialization, no interaction from host is required
- Atomic Rules implementation of a Gardner Type-2 Digital Phase Locked Loop (DPLL)
  - Double-Precision Floating-Point implementation
  - Sample Rate $F_{sample} = 1\ Hz$
  - Nyquist Rate $F_{Nyquist} = 0.5\ Hz$
  - Damping (zeta) $\xi = 1.0$
  - Noise Bandwidth $\omega_{BW} = 0.1\ Hz$
  - Natural Frequency $\omega_n = 0.025\ Hz$
  - Tau τ= 10 Seconds
- FPGA Resources Used (Includes TimeServo and Other Sub-Cores)
  - ALMs/LUTs: 13K
  - M20Ks/BRAMs: 17
  - DSPs: 6

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