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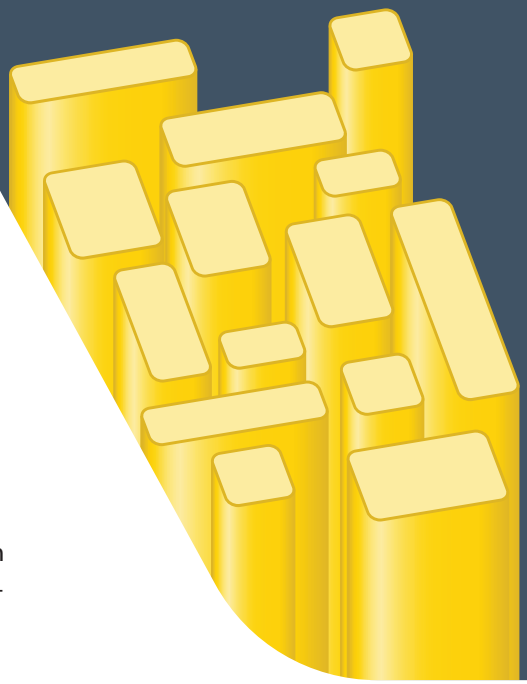
Partner Solution



Arkville

DPDK/AXI Aware Data Mover IP Core

Seamlessly transport data between FPGA logic and host memory at up to 60 GBytes/s (480 Gbps) in each direction.

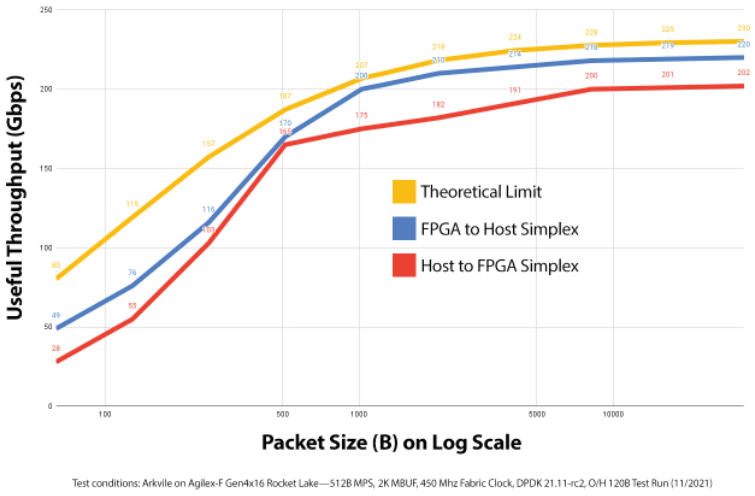
Arkville provides a high-throughput, low-latency conduit between host memory and FPGA fabric logic, offloading CPU core usage, eliminating memory copies, and improving overall efficiency.

Software engineers see industry-standard APIs for producing and consuming data in zero-copy user space memory buffers on the host. Hardware engineers see industry-standard RTL interfaces to produce and consume the same data.

Up to 480Gbps
PCIe Gen5

Any line rate up to 400GbE

DPDK & AXI Standards

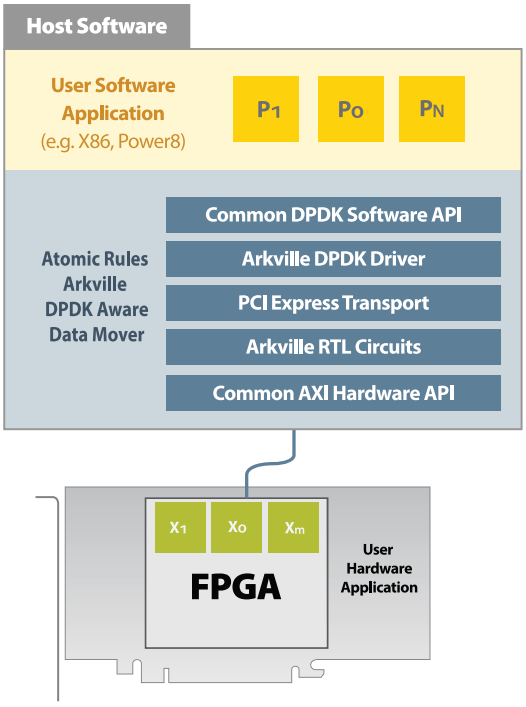


Arkville PCIe Gen4 x16 Throughput in Gbps

Features

- Offload server cycles to FPGA gates
- Bring your FPGA-based packet processing solutions to market quickly
- Future proof your GPP/FPGA application with the DPDK and AXI standards
- Line rate agnostic: 0perates at any line rate, including 1/5/10/25/40/50/100/400 GbE
- Up to 480 Gbps and 500 Mpps with Gen5 x16 interface
- FPGA vendor agnostic RTL
- Support for both Intel/PSG and AMD/Xilinx FPGA devices
- Open-source "net/ark" Arkville driver in DPDK 23.11

Arkville
Data Mover IP Core



Product Operation

As shown in the block diagram, Arkville has both a hardware and software component. The hardware component is an IP core that resides in the FPGA, producing and consuming AXI streams of packets making ingress or egress. The software component is a DPDK PMD "net/ark", the Arkville DPDK poll-mode driver. Arkville is a conduit between FPGA logic and Host user memory for bulk data movement or individual packets.

Together, an Arkville solution looks to software like a "vanilla" line rate agnostic FPGA-based NIC (without any specific MAC). DPDK applications do not need to change significantly in order to enjoy the advantages of FPGA hardware acceleration.

Detailed Feature List

Overall

- Ready-to-go solution to FPGA/GPP packet movement
- 4 physical queue-pairs (RX/TX) standard; up to 128 physical queue-pairs
- Single PCIe Physical Function (PF) supporting multiple ports
- Concurrent, full-duplex upstream and downstream data movement

GPP/Software Specific

- DPDK Arkville PMD in DPDK 23.11
- Tested extensively with Jenkins CI/CD
- Unencumbered Application BAR (ABAR) for FPGA application

FPGA/Hardware Specific

- AXI Streaming interfaces for packet movement
- Up to 1 Tbps burst traffic (two 128 Byte wide, 500 MHz, AXI streams)
- Dedicated Application BAR (ABAR) AXI4-master for the FPGA application

Reference Examples

Atomic Rules provides Arkville example designs that may be used as a starting point for your own solutions. These include:

- Four-port, four-queue 10 GbE example (Arkville + 4×10 GbE MAC)
- Single-port, single-queue 100 GbE example (Arkville + 1×100 GbE MAC)

Sample Implementation Results

Device	Speed	ALMs	FFs	M20k	Fmax
Intel Agilex F-Series	-2	81K	220K	250	500

Compatible FPGA Cards

- IA-840F
- IA-420F

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