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Partner IP

Atomic Rules

Arkville DPDK
IP Core

DPDK/AXI Aware Data Mover IP Core

intel

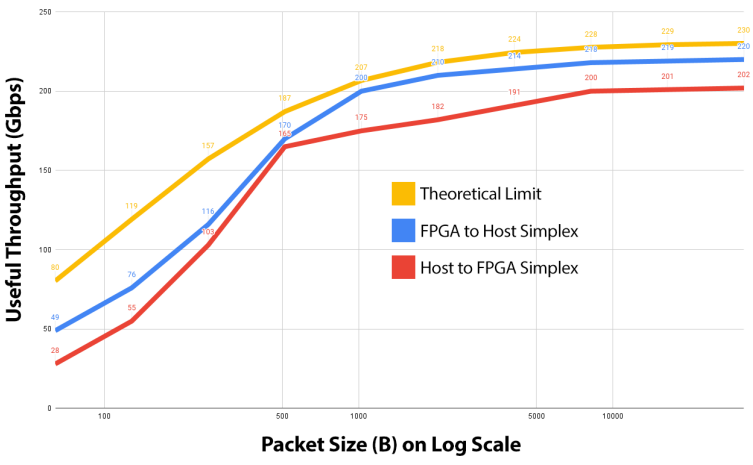
intel
AGILEX

Computational packet processing applications such as software-defined networking (SDN), network functions virtualization (NFV), machine learning, video transcoding, image and speech recognition, CloudRAN, and Big Data analytics may employ both wirespeed gateware functions on an FPGA in conjunction with fast operations performed in software on one or more host processor cores.

Arkville DPDK IP core from Atomic Rules provides a high throughput line-rate agnostic conduit between FPGA hardware and GPP software. Using industry-standard AXI interfaces on the FPGA side and DPDK interfaces on the software API/ABI side, Arkville provides an exceptional "out-of-the-box" solution for both hardware and software teams. Because Arkville was designed with the specific goal of accelerating and empowering DPDK, the performance is significantly higher than one of a naïve DMA implementation on an FPGA.

key features

- up to **220Gbps** with **PCIe Gen 4**
- Operate at any line rate up to **400GbE**
- **DPDK** and **AXI** standards



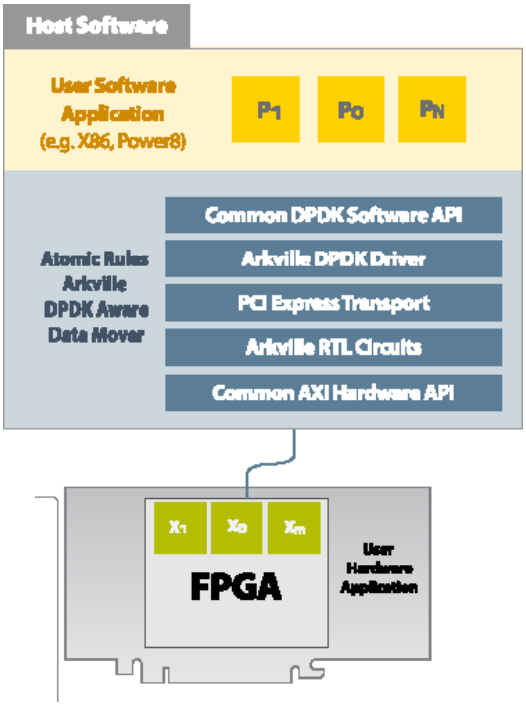
Test conditions: Arkvile on Agilex-F Gen4x16 Rocket Lake—512B MPS, 2K MBUF, 450 Mhz Fabric Clock, DPDK 21.11-rc2, O/H 120B Test Run (11/2021)

Features

- Offload server cycles to FPGA gates
- Bring your FPGA-based packet processing solutions to market quickly
- Future proof your GPP/FPGA application with the DPDK and AXI standards
- Line rate agnostic: Operates at any line rate, including 1/5/10/25/40/50/100/400 GbE
- Up to 220 Gbps and 500 Mpps with Gen4x16 interface
- 4 Physical Queue-Pairs (RX/TX) Standard; Up to 128 Physical Queue-Pairs
- Open-Soruce "net/ark/ Arkville driver in DPDK 21.11

Arkville DPDK

IP Core



Product Operation

As shown in the block diagram, Arkville has both a hardware and software component. The hardware component is an IP core that resides in the FPGA, producing and consuming AXI streams of packets making ingress or egress. The software component is a DPDK PMD "net/ark", the Arkville DPDK poll-mode driver. Arkville is a conduit between FPGA logic and Host user memory for bulk data movement or individual packets.

Together, an Arkville solution looks to software like a "vanilla" line rate agnostic FPGA-based NIC (without any specific MAC). DPDK applications do not need to change significantly in order to enjoy the advantages of FPGA hardware acceleration.

Detailed Feature List

Overall

- Ready-to-Go Solution to FPGA/GPP Packet Movement
- 4 Physical Queue-Pairs (RX/TX) Standard; Up to 128 Physical Queue-Pairs
- Single PCIe Physical Function (PF) supporting multiple ports
- Concurrent, Full-Duplex Upstream and Downstream Data Movement

GPP/Software Specific

- DPDK Arkville PMD in DPDK 21.11
- Tested extensively in with DPDK Test Suite (DTS)
- Unencumbered Application BAR (ABAR) for FPGA Application

FPGA/Hardware Specific

- AXI Streaming interfaces for packet movement
- Up to 512 Gbps, 1 Gpps burst traffic (Two 64 Byte wide, 500 MHz, AXI streams)
- Dedicated Application BAR (ABAR) AXI4-Master for the FPGA Application
- Integrated with Intel Quartus™ 21.3

Reference Examples

Atomic Rules provides Arkville example designs that may be used as a starting point for your own solutions. These include:

- Four-Port, Four-Queue 10 GbE example (Arkville + 4×10 GbE MAC)
- Single-Port, Single-Queue 100 GbE example (Arkville + 1×100 GbE MAC)

Sample Implementation Results

Device	Speed	ALMs	FFs	BRAM	Fmax
Intel Agilex F-Series	-2	100k	100k	100	500

Compatible FPGA Cards

- IA-840F
- IA-420F

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Rev 2021.11.22 | November 2021

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