

BittWare XUP-VV8 PCIe Card >

The BittWare XUP-VV8 offers a large AMD FPGA in a 3/4-length PCIe board featuring QSFP-DD (double-density) cages for maximum port density.

Using the Virtex UltraScale+ VU13P or VU9P FPGA, the board supports up to 8x 100GbE or 32x 10/25GbE. The FPGA provides large logic and memory resources—up to 3.8M logic cells and 455Mb embedded memory. The board also provides a jitter cleaner to support synchronous ethernet. The board can be configured as single width for users who don't need external memory on the DIMMs.



Breakout QSFP28 to 2x 100GbE modules

Module connects to one of the QSFP-DD cages on XUP-VV8

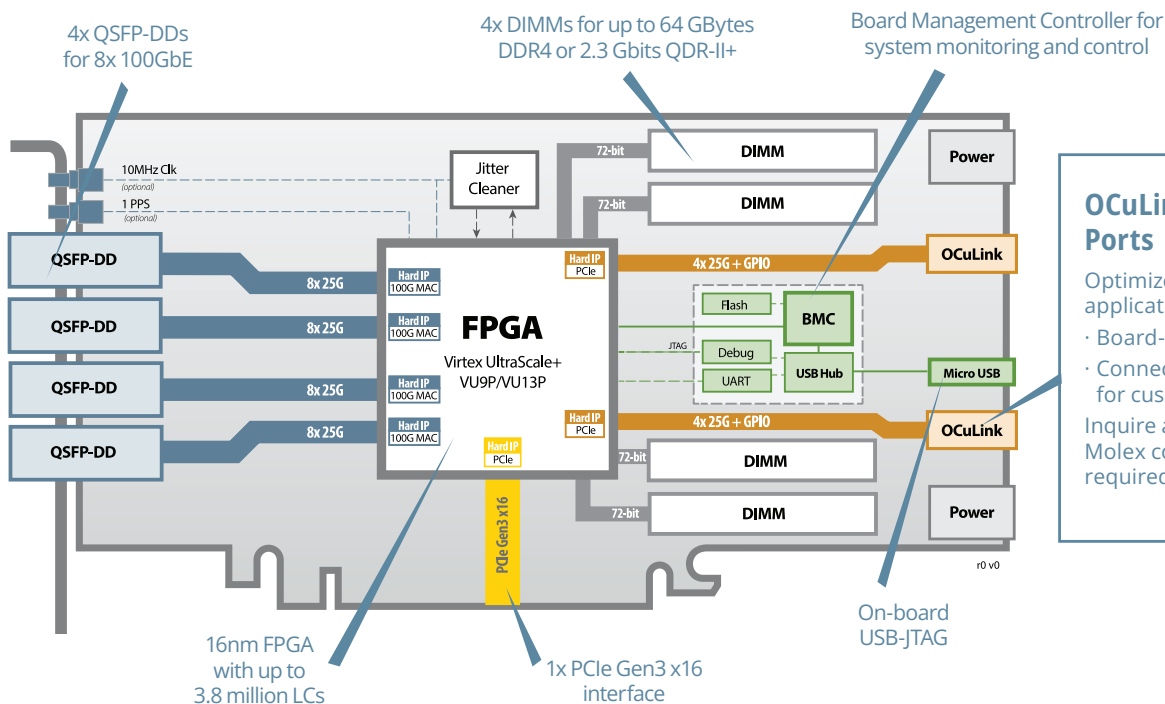
FEATURES AND ADVANTAGES

8x 100GbE via 4 QSFP-DD
Ideal for network-intensive applications

Up to 64 GBytes DDR4
Large pool of off-chip memory

Up to VU13P: 3.8million LCs
FPGA by AMD
Powerful FPGA resources

Expansion options
OCuLink for accessory boards or board-to-board interconnect



OCuLink Expansion Ports

Optimize the XUP-VV8 for your application with expansion:

- Board-to-board interconnect
- Connect to accessory boards for customization options

Inquire about customized Molex connectors/cables as required for your application.

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SYSTEM SPECIFICATIONS

FPGA

- Virtex UltraScale+
 - VU9P or VU13P in D2104 package
 - Core speed grade - 2
- Contact us for other FPGA options

On-board Flash

- Flash memory for booting FPGA

External memory

- 4 DIMM sites, each supporting:
 - Up to 16 GBytes DDR4 x72 with ECC
 - Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks)

Host interface

- x16 Gen3 interface direct to FPGA

USB port

- Micro USB: access to BMC, FPGA JTAG, and FPGA UART

Timestamp

- 1 PPS input and 10MHz clock input

OCuLink

- 2 OCuLink on rear edge, each connected to FPGA via 4x GTY transceivers

QSFP cages

- 4 QSFP-DD cages on front panel
- Each supports 2x 100GbE, 2x 40GbE, 8x 25GbE, or 8x 10GbE
- Jitter cleaner for network recovered clocking

Board

Management Controller

- Voltage, current, temperature monitoring
- Power sequencing and reset
- Field upgrades
- FPGA configuration and control
- Clock configuration
- I²C bus access
- USB 2.0
- Voltage overrides

Cooling

- Standard: dual-width passive heatsink
- Optional: single-width passive heatsink*

Electrical

- On-board power derived from 12V PCIe slot & two AUX connectors (8-pin)
- Power dissipation is application dependent

Environmental

- Operating temperature 5°C to 35°C

Form factor

- ¾-length, standard-height PCIe dual-width board
- Single-width option*
- 111.15mm x 254.00mm (4.376in x 10.000in)

DEVELOPMENT TOOLS

System development

- **BittWorks II Toolkit** - host, command, and debug tools for BittWare hardware

FPGA development

- **FPGA Examples** - example Vivado projects, available with the BittWorks II Toolkit
- **AMD Tools** - Vivado® Design Suite

SAFETY & COMPLIANCE

- FCC (USA) 47CFR15.107 / 47CFR15.109
- CE (Europe) EN55032:2015 / EN55035:2017
- UKCA (United Kingdom) BS EN55032:2015 / BS EN55035:2017
- ICES (Canada) ICES-003 Issue 6 January 2016
- RoHS: Directive 2011/65/EU of the European Parliament and of the Council of 8 June 2011 on the restriction of the use of certain hazardous substances in electrical and electronic equipment



Embedded
Partner
Network

PLATINUM

To learn more, visit bittware-molex.com

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