BittWare a molex company

XUP-PL4

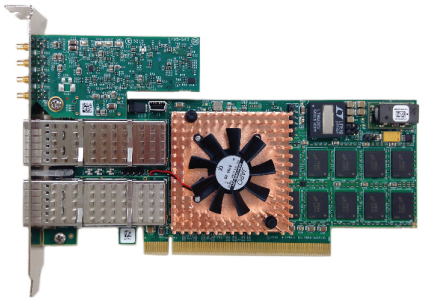
PCIe FPGA Board

UltraScale+ PCIe board with QSFP and DDR4

BittWare's XUP-PL4 is a low-profile PCIe x16 card based on the AMD Virtex UltraScale+ FPGA. The UltraScale+ devices deliver high-performance, high-bandwidth, and reduced latency for systems demanding massive data flow and packet processing. The board offers up to 32 GBytes of memory, sophisticated clocking and timing options, and two front panel QSFP cages, each supporting up to 100 Gbps (4x25) - including 100GbE.

The XUP-PL4 also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform integration and management. All of these features combine to make the XUP-PL4 ideal for a wide range of data center applications, including network processing and security, acceleration, storage, broadcast, and SigInt.

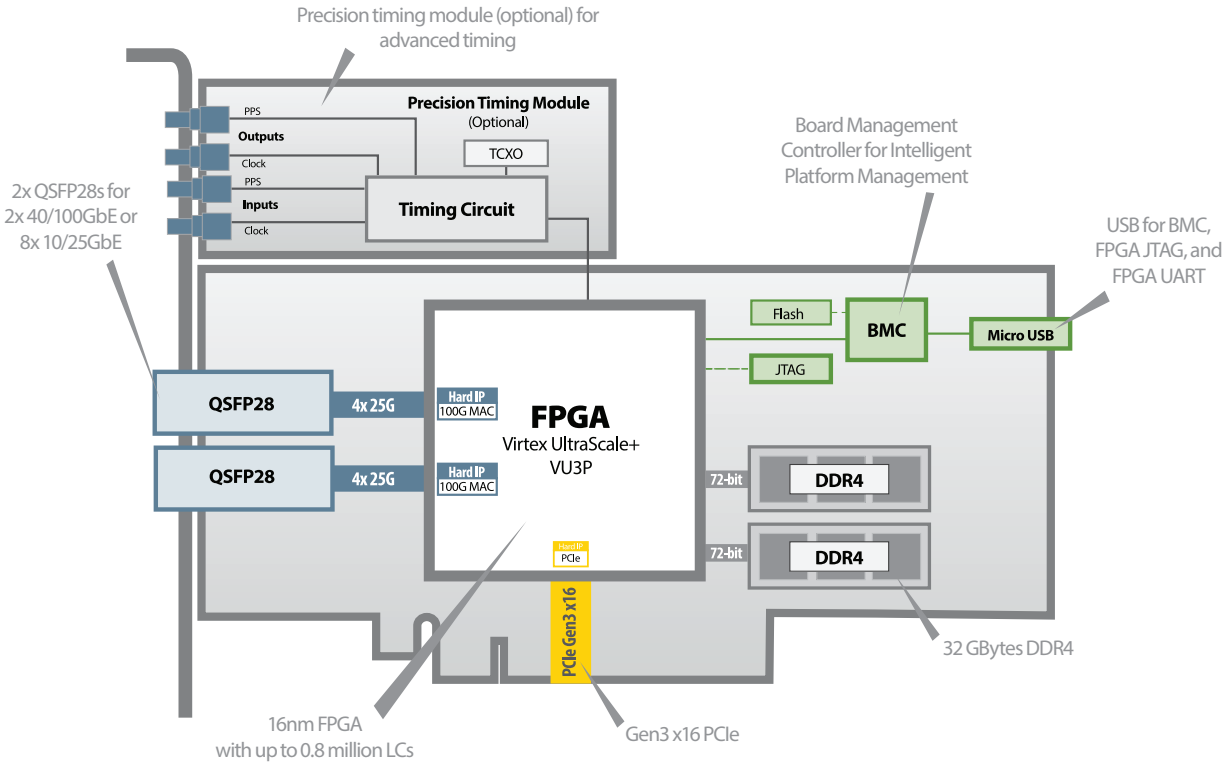
AMD



An optional add-on module provides precision timestamping capabilities

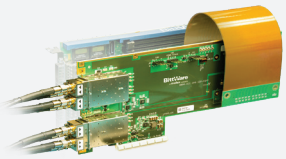
key features

- **2x 100GbE** via 2 QSFP28
- Up to **32 GBytes** DDR4
- Precision **clocking** and **timing** options



Additional Services

Take advantage of BittWare's range of design, integration, and support options

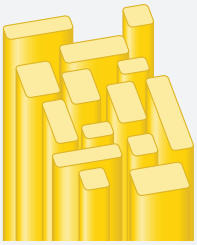


Customization

Additional specification options or accessory boards to meet your exact needs.

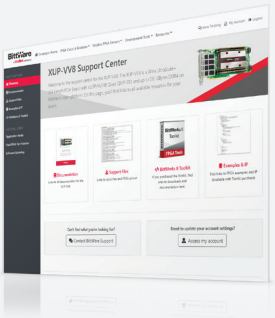
Server Integration

Available pre-integrated in our TeraBox servers in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	• Virtex UltraScale+
	  • VU3P in C1517 package
	  • Core speed grade - 2
	• Contact BittWare for other FPGA options

On-board memory	• Flash memory for booting FPGA • Two banks of up to 16 GB DDR4 (x72)
Host interface	• x16 Gen3 interface direct to FPGA
Utility header	• Micro USB for BMC access and programming Flash
Timestamping (optional)	• 1 PPS input/output • Reference clock input/output
QSFP cages	• 2 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 8 transceivers • Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE and can be combined for 400GbE
Board Management Controller	• Voltage, current, temperature monitoring • Power sequencing and reset • Field upgrades • FPGA configuration and control • Clock configuration • I^2C bus access • USB 2.0 • Voltage overrides
Cooling	• Standard: single-width active heatsink
Electrical	• On-board power derived from 12V PCIe slot • Power dissipation is application dependent
Environmental	• Operating temperature 5°C to 35°C
Size	• Low profile (half-height, half-length) PCIe slot board • 68.90mm x 167.65mm (2.713in x 6.600in)

Development Tools

System development	• BittWorks II Toolkit - host, command, and debug tools for BittWare hardware
FPGA development	• FPGA Examples - example Vivado projects • AMD Tools - Vivado® Design Suite

To learn more, visit **www.BittWare.com**

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