

**BittWare**  
a molex company

**XUP-P3R**  
PCIe FPGA Card



## UltraScale+ PCIe board with Quad QSFP and 512 GBytes DDR4

BittWare's XUP-P3R is a 3/4-length PCIe x16 card based on the AMD Virtex UltraScale+ FPGA. The UltraScale+ devices deliver high-performance, high-bandwidth, and reduced latency for systems demanding massive data flow and packet processing. The board offers extensive memory configurations supporting up to 512 GBytes of memory, sophisticated clocking and timing options, and four front panel QSFP cages, each supporting up to 100 Gbps (4x25) - including 100GbE.

The XUP-P3R also incorporates a Board Management Controller (BMC) for advanced system monitoring, which greatly simplifies platform integration and management. All of these features combine to make the XUP-P3R ideal for a wide range of data center applications, including network processing and security, acceleration, storage, broadcast, and SigInt.



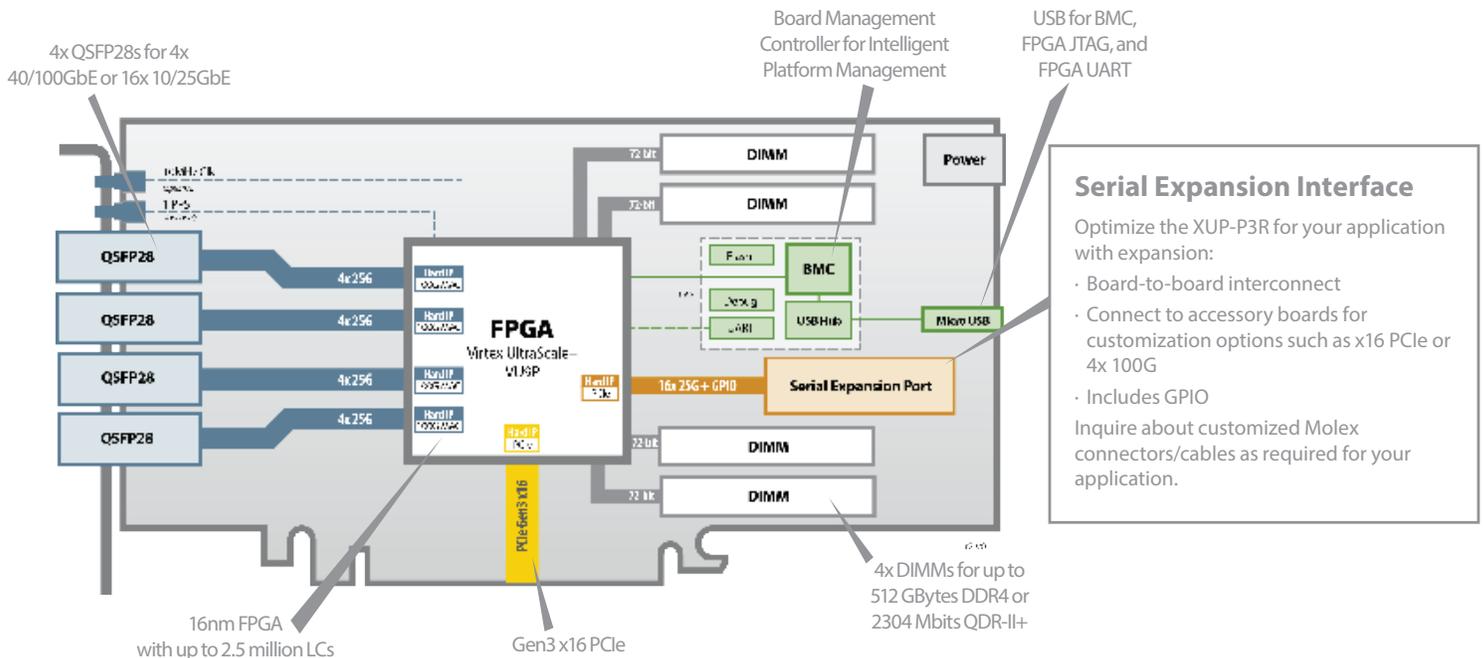
Optional accessory boards provide customization options such as x16 PCIe, 4x 100G, or video transceivers.

### key features

**4x 100GbE**  
via 4 QSFP28

**Up to 512 GBytes**  
DDR4

**Up to VU9P:**  
**2.5 million LCs**  
FPGA by AMD



# Additional Services

Take advantage of BittWare's range of design, integration, and support options



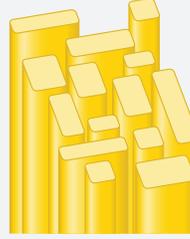
## Customization

[Additional specification options](#) or [accessory boards](#) to meet your exact needs.



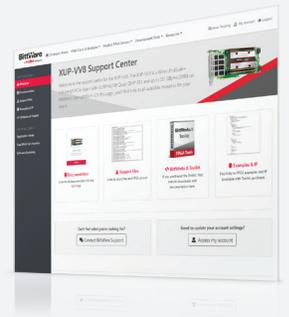
## Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



## Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



## Service and Support

BittWare Developer Site provides online documentation and issue tracking.

## Board Specifications

FPGA	<ul style="list-style-type: none"> <li>Virtex UltraScale+             <ul style="list-style-type: none"> <li>VU9P</li> <li>Core speed grade - 2</li> </ul> </li> <li>Contact BittWare for additional FPGA options</li> </ul>
External memory	<ul style="list-style-type: none"> <li>4 DIMM sites, each supporting*:             <ul style="list-style-type: none"> <li>Up to 128 GBytes DDR4 x72 with ECC</li> <li>Up to 576 Mbits dual QDR-II+ x18 (2 independent 288 Mbit banks)</li> </ul> </li> </ul>
Host interface	<ul style="list-style-type: none"> <li>x16 Gen3 interface direct to FPGA</li> </ul>
USB header	<ul style="list-style-type: none"> <li>Micro USB: (USB 2.0) for debug and programming FPGA and Flash</li> </ul>
Serial expansion port (SEP)	<ul style="list-style-type: none"> <li>Expansion interface to FPGA via 20x GTY transceivers (optional; requires second slot)</li> <li>14x GPIO signals to the FPGA</li> </ul>
QSFP cages	<ul style="list-style-type: none"> <li>4 QSFP28 (zQSFP) cages on front panel connected directly to FPGA via 16 transceivers</li> <li>Each supports 100GbE, 40GbE, 4x 25GbE, or 4x 10GbE and can be combined for 400GbE</li> </ul>
On-board Flash	<ul style="list-style-type: none"> <li>Flash memory for booting FPGA</li> </ul>

\*DIMM sites 1/2 and sites 3/4 must have the same memory type, or be empty.

Board Management Controller	<ul style="list-style-type: none"> <li>Voltage, current, temperature monitoring</li> <li>Power sequencing and reset</li> <li>Field upgrades</li> <li>FPGA configuration and control</li> <li>Clock configuration</li> <li>I<sup>2</sup>C bus access</li> <li>USB 2.0</li> <li>Voltage overrides</li> </ul>
Cooling	<ul style="list-style-type: none"> <li>Standard: double-width active fan and heatsink</li> <li>Optional: double-width passive heatsink</li> <li>Optional: double-width advanced passive cooling with heatpipes</li> </ul>
Electrical	<ul style="list-style-type: none"> <li>On-board power derived from 12V PCIe slot &amp; an AUX connector (6-pin)</li> <li>Power dissipation is application dependent</li> </ul>
Environmental	<ul style="list-style-type: none"> <li>Operating temperature 5°C to 35°C</li> </ul>
Size	<ul style="list-style-type: none"> <li>¾-length, standard-height PCIe dual-slot card</li> <li>111.15mm x 241.30mm (4.376in x 9.500in)</li> </ul>
MPN	<ul style="list-style-type: none"> <li>XUPP3R-0072</li> </ul>

## Development Tools

System development	<ul style="list-style-type: none"> <li><a href="#">BittWorks II Toolkit</a> - host, command, and debug tools for BittWare hardware</li> </ul>
FPGA development	<ul style="list-style-type: none"> <li><a href="#">FPGA Examples</a> - example Vivado projects, available with the BittWorks II Toolkit</li> <li><a href="#">AMD Tools</a> - Vivado® Design Suite</li> </ul>

## Safety & Compliance

- FCC (USA) 47CFR15.107 / 47CFR15.109
- CE (Europe) EN55032:2015/A11:2020 / EN55024:2010 / EN55035:2017 / EN61000-3-2:2014 / EN610003-3:2013
- UKCA (United Kingdom) BS EN55032:2012/AC:2013 / BS EN55024:2010 / BS EN55035:2017 / BS EN61000-3-2:2014 / BS EN610003-3:2013
- ICES (Canada) ICES-003 Issue 7
- The safety objectives referred to in Article 3 and set out in Annex I of DIRECTIVE 2014/35/EU have been fulfilled
- RoHS compliant to the 2011/65/EU + 2015/863 directive



To learn more, visit [www.BittWare.com](http://www.BittWare.com)

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