molex

BittWare IA-860m PCIe Card ›

The BittWare IA-860m is an Altera Agilex™ M-series FPGA card optimized for throughput- and memory-intensive applications.

The M-series FPGA features an extensive memory hierarchy including integrated high-bandwidth memory (HBM2e) and a hard memory Network-on-Chip (NoC) to maximize memory bandwidth. The IA-860m card provides a balance of I/O and memory leveraging the Agilex chip's unique tiling architecture with QSFP-DDs, PCIe Gen5 x16 with CXL support, and optional MCIO expansion port for a variety of applications.

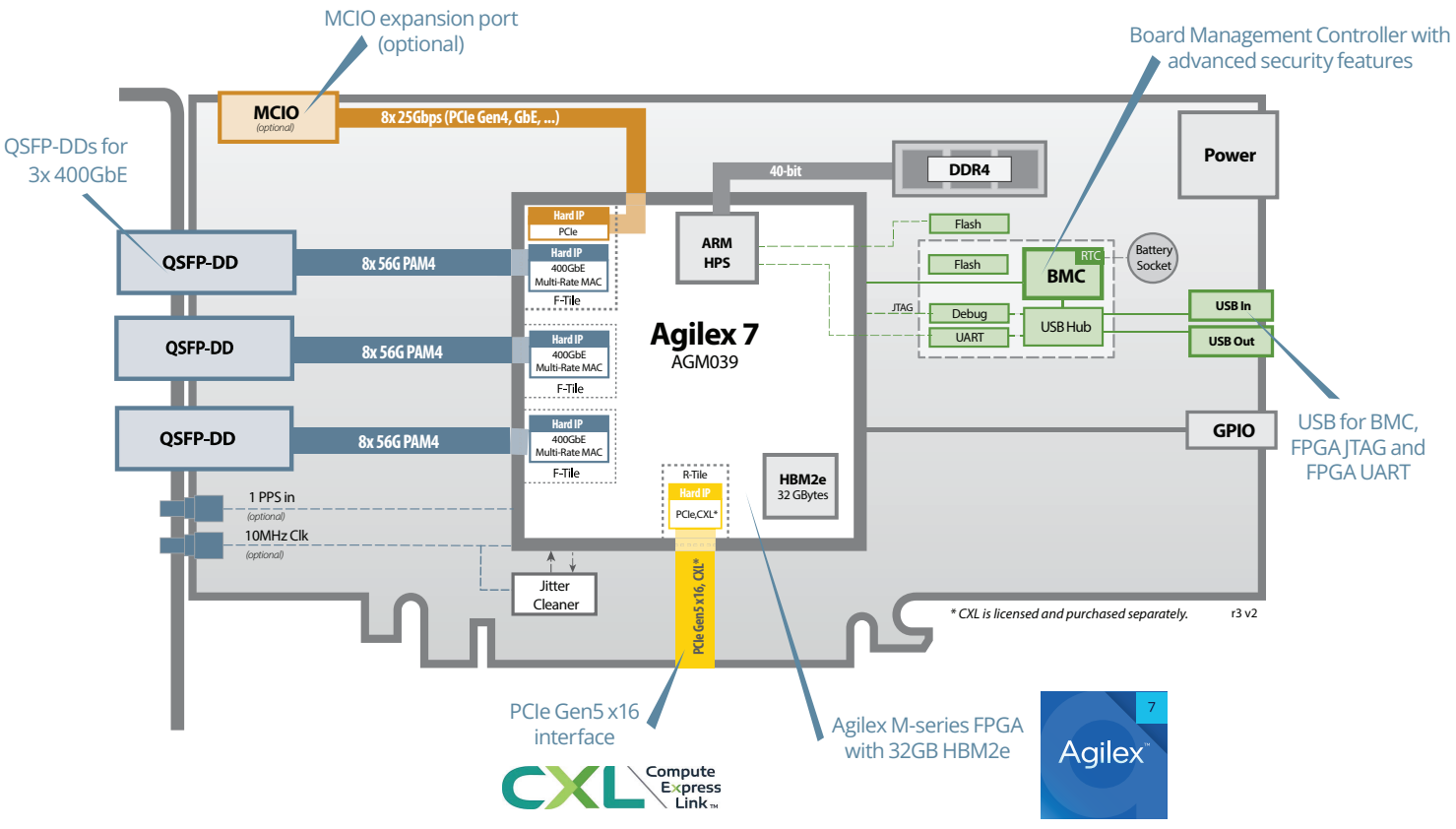
FEATURES AND ADVANTAGES

3x 400GbE, 12x 100G or 24x 10/25/50G
Ideal for network-intensive applications

32GB HBM2e memory
Large pool of high-bandwidth on-chip memory

Altera Agilex M-Series FPGA
Powerful FPGA resources with 3.8m LEs

PCIe Gen5 with support for CXL
High-speed, low-latency host interface



PRODUCT OVERVIEW SHEET

BittWare IA-860m PCIe Card

BOARD SPECIFICATIONS

FPGA
- Altera Agilex 7 M-Series: AGM039 (default)
  - Package: R47A
  - 32GB HBM2e
  - Core speed grade -2; XCVR speed grade -1
  - CXL with XCVR speed grade -1 (CXL IP is licensed and purchased separately)
  - FPGA includes ARM HPS

ARM HPS
- Dedicated 40-bit DDR4
- Dedicated Flash memory for booting ARM

On-board Flash
- 2Gbit Flash memory for booting FPGA

Host interface
- x16 PCIe Gen5 interface direct to FPGA
- CXL support (CXL IP is licensed and purchased separately)

QSFP-DD cages
- 3x QSFP-DD cages on front panel connected directly to FPGA via 24 transceivers
- User programmable low jitter clocking supporting 10/25/40/100/200/400GbE
- Each QSFP-DD can be independently clocked
- Jitter cleaner for network recovered clocking
- Multi-rate hard MAC+FEC
- Fully backward compatible with QSFP28s

MCIO
- x8 connector supporting 2x Gen4 x4 root complexes (optional)

GPIO
- 4x GPIO

USB
- USB access to BMC, USB-JTAG, USB-UART

Board Management Controller
- Power sequencing and reset
- Voltage, current, temperature monitoring
  - Protection shut-down
- Clock configuration
- Low bandwidth BMC-FPGA comms with SPI link
- USB 2.0
- PLDM support
- Card-level security
  - BMC Root of Trust
  - BMC and FPGA secure boot
  - BMC and FPGA secure upgrade
  - Key management
- RTC with battery backup

Cooling
- Standard: dual-width passive heatsink
- Optional: dual-width liquid cooling

Electrical
- On-board power derived from PCIe slot 12V and 12-pin AUX power connector
- Power dissipation is application dependent
- Typical max power consumption TBD

Environmental
- Operating temperature: 5°C to 35°C (passive heatsink)

Quality
- Manufactured to IPC-A-610 Class 2
- RoHS compliant
- CE, FCC, UKCA & ICES approvals

Form factor
- Standard-height, full-length, dual-slot PCIe card
- 111.15mm x 312.00mm (4.376in x 12.283in)

ACCESSORY CABLES

Access to USB andJTAG requires accessory cables. **Cables are sold separately.**

USB In cable	Pico-lock to USB A cable Part number: RS-PL05-UAP-83 Designed for deployment in servers
USB out cable	Pico-lock to Pico-lock Part number: RS-PL05-PL05-24
JTAG-only cable	Pico-lock to JTAG cable Part number: RS-PL06-JTB-13 Recommended for development

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DEVELOPMENT TOOLS

System development
BittWare SDK including libraries and board monitoring utilities

Application development
Supported design flows - Altera High-Level Synthesis (C/C++) and Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

SAFETY & COMPLIANCE

- FCC (USA) 47CFR15.107 / 47CFR15.109
- CE (Europe) EN55032:2015 + A1:2020 / EN55035:2017
- UKCA (United Kingdom) BS EN55032:2015 + A1:2020 / BS EN55035:2017
- ICES (Canada) ICES-003 Issue 7
- Safety: CB Test Certified EN IEC 62368-1:2020+A11:2020 / BS EN IEC 62368-1:2020+A11:2020 / CSA/UL 62368-1:2019 with national differences for EU Group, United States and Canada
- RoHS compliant

To learn more, visit **bittware-molex.com**

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