



Agilex™ FPGA card featuring 400G and Gen5 PCle

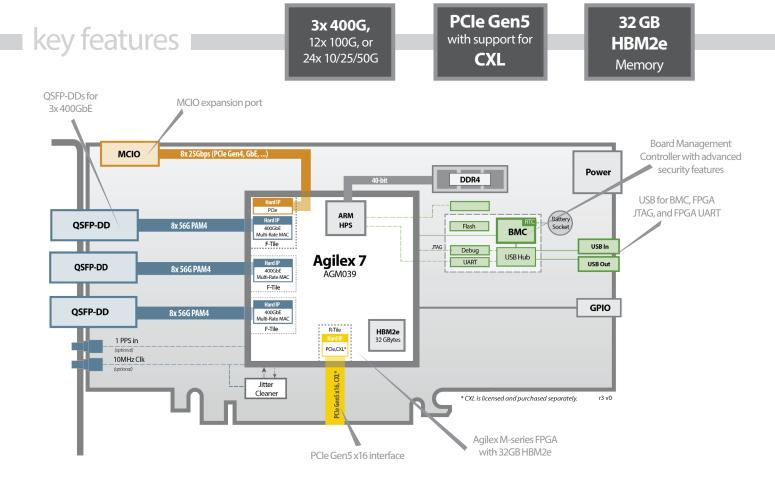
M-series FPGA with HBM2e supporting 1TBps total memory bandwidth

BittWare's IA-860m is an Altera Agilex™ M-series FPGA card optimized for throughputand memory-intensive applications. The M-series FPGA features an extensive memory hierarchy including integrated high-bandwidth memory (HBM2e) and a hard memory Network-on-Chip (NoC) to maximize memory bandwidth. The IA-860m card provides a balance of I/O and memory leveraging the Agilex chip's unique tiling architecture with QSFP-DDs, PCIe Gen5 x16 with CXL support, and MCIO expansion port for a variety of applications. intel.
AGILEX

oneAPI

Compute

The IA-860m has support for Intel oneAPI™, which enables an abstracted development flow for dramatically simplified code re-use across multiple architectures.



IA-860m PCle FPGA Card

Board Specifications

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FPGA	Altera Agilex 7 M-Series: AGM039 (default) Package: R47A 32GB HBM2e Core speed grade -2; XCVR speed grade -1 CXL with XCVR speed grade -1 (CXL IP is licensed and purchased separately) FPGA includes ARM HPS
ARM HPS	Dedicated 40-bit DDR4Dedicated Flash memory for booting ARMOptional 1GbE interface (contact BittWare)
On-board Flash	2Gbit Flash memory for booting FPGA
Host interface	 x16 PCle Gen5 interface direct to FPGA CXL support (CXL IP is licensed and purchased separately)
QSFP-DD cages	 3x QSFP-DD cages on front panel connected directly to FPGA via 24 transceivers User programmable low jitter clocking supporting 10/25/40/100/200/400GbE Each QSFP-DD can be independently clocked Jitter cleaner for network recovered clocking Multi-rate hard MAC+FEC Fully backward compatible with QSFP28s
MCIO	x8 connector supporting 2x Gen4 x4 root complexes
GPIO	• 4x GPIO
External clocking	1 PPS and 10MHz ref clk front panel inputs (optional)
USB	USB access to BMC, USB-JTAG, USB-UART

Accessory Cables

Access to USB and JTAG requires accessory cables. Cables are sold separately.

USB In cable	Pico-lock to USB A cable BittWare part number: RS-PL05-UAP-83 Designed for deployment in servers
USB Out cable	Pico-lock to Pico-lock BittWare part number: RS-PL05-PL05-24
JTAG-only cable	Pico-lock to JTAG cable BittWare part number: RS-PL06-JTB-13 Recommended for development

Board Management Controller	Power sequencing and reset Voltage, current, temperature monitoring Protection shut-down Clock configuration Low bandwidth BMC-FPGA comms with SPI link USB 2.0 PLDM support Card-level security BMC Root of Trust BMC and FPGA secure boot BMC and FPGA secure upgrade Key management RTC with battery backup
Cooling	Standard: dual-width passive heatsink Optional: dual-width liquid cooling
Electrical	 On-board power derived from PCle slot 12V and 12-pin AUX power connector Power dissipation is application dependent Typical max power consumption TBD
Environmental	Operating temperature: 5°C to 35°C (passive heatsink)
Quality	 Manufactured to IPC-A-610 Class 2 RoHS compliant CE, FCC, UKCA & ICES approvals
Form factor	Standard-height, full-length, dual-slot PCle card 111.15mm x 312.00mm (4.376in x 12.283in)

Development Tools

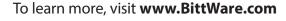
System development	BittWare SDK including PCle driver, libraries, and board monitoring utilities
Application development	Supported design flows - Altera FPGA oneAPI Base Toolkit, Altera High-Level Synthesis (C/C++) and Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

Safety & Compliance

- FCC (USA) 47CFR15.107 / 47CFR15.109
- CE (Europe) EN55032:2015 / EN55035:2017 / EN61000-3-2:2019 + A1:2021 / EN610003-3:2013
- UKCA (United Kingdom) BS EN55032:2015 / BS EN55035:2017 / BS EN61000-3-2:2019 +
- ICES (Canada) ICES-003 Issue







r3 v1 | last revised 2025.05.28

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