



Agilex™ FPGA card with 3x QSFP-DDs

3x 200GbE with up to 128GBytes DDR4 SDRAM

BittWare's IA-840f is an Altera Agilex™-based FPGA card designed to deliver up to 40% higher performance for data center, networking and edge compute workloads. BittWare maximized I/O features on the card using the Agilex chip's unique tiling architecture with three QSFP-DDs (3× 200G) and PCIe Gen4 x16. The card also supports Intel oneAPI™, which enables an abstracted development flow for dramatically simplified code re-use across multiple architectures.

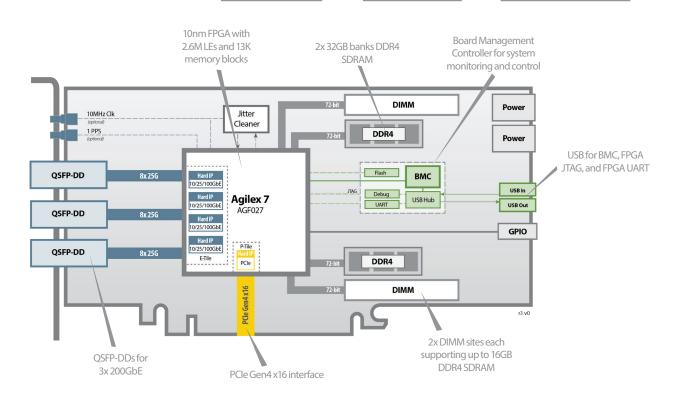


The IA-840f supports Intel's OneAPI open standardsbased unified programming model

key features



Intel OneAPI support Altera Agilex™ FPGA with up to **2.6M Logic Elements**



Additional Services

Take advantage of BittWare's range of design, integration, and support options



Customization

Additional specification options or accessory boards to meet your exact needs.



Server Integration

Available pre-integrated in our <u>TeraBox servers</u> in a range of configurations.



Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

FPGA	 Altera Agilex 7 F-Series AGF027 in an R2581A package Core speed grade -2: I/O speed grade -2 Contact BittWare for other Agilex FPGA options
On-board Flash	2Gbit Flash memory for booting FPGA
External memory	 2x 288-pin DIMM slots, each supporting up to 16GE DDR4 SDRAM modules (up to 32GB total) 2x banks on-board DDR4, up to 32GB each
Host interface	x16 Gen4 interface direct to FPGA, connected to PCIe hard IP
QSFP-DD cages	 3 QSFP-DD cages on front panel connected directly to FPGA via 24 transceivers User programmable low jitter clocking supporting 10/25/40/100GbE Each QSFP-DD can be independently clocked Jitter cleaner for network recovered clocking Multi-rate hard MAC+FEC for 10/25/100GbE (4x HardIP) Fully backward compatible with QSFP28s
External clocking	1 PPS and 10MHz ref clk front panel inputs (optional)
USB	USB access to BMC, USB-JTAG, USB-UART
Board Management Controller	 Voltage, current, temperature monitoring Power sequencing and reset Field upgrades FPGA configuration and control Clock configuration Low bandwidth BMC-FPGA comms with SPI link USB 2.0 PLDM support Voltage overrides

		7
Ac	gilex	<u>, </u>



Cooling	Standard: dual-slot passive heatsinkOptional: dual-slot liquid cooling
Electrical	 On-board power derived from PCle slot 12V and two AUX connectors Power dissipation is application dependent Typical max power consumption 225W
Environmental	• Operating temperature: 5°C to 35°C
Quality	 Manufactured to IPC-A-610 Class 2 RoHS compliant CE, FCC, UKCA & ICES approvals
Form factor	 Standard-height, dual-slot PCle card 111.15mm x 266.70mm (4.376in x 10.500in)

Development Tools

System development	BittWare SDK including PCIe driver, libraries, and board monitoring utilities
Application development	Supported design flows - Intel FPGA oneAPI Base Toolkit, Intel High-Level Synthesis (C/C++) and Quar- tus Prime Pro (HDL, Verilog, VHDL, etc.)

Safety & Compliance

- FCC (USA) 47CFR15.107 / 47CFR15.109
- CE (Europe) EN55032:2015 / EN55035:2017 / EN61000-3-2:2019 + A1:2021 / EN610003-3:2013 + A1:2019
- UKCA (United Kingdom) BS EN55032:2015 / BS EN55035:2017 / BS EN61000-3-2:2019 + A1:2021 / BS EN610003-3:2013 + A1:2019
- ICES (Canada) ICES-003 Issue 7
- RCM (Aus/NZ)
- Safety: CE (Europe) EN IEC 62368-1:2018 / EN IEC 62368-1:2020 + A11:2020 with national differences for Australia, New Zealand, EU Group, Singapore, United States, Canada and UK
- Safety: AS/NZS 62368-1:2022
- Safety: CSA/UL 62368-1:2019
- Safety: UKCA (United Kingdom) BS EN IEC 62368-1:2018 / BS EN IEC 62368-1:2020 +A11:2020
- CB Scheme Certificate No. DK-141340-UL
- RoHS compliant to the 2011/65/EU + 2015/863 directive

To learn more, visit www.BittWare.com

r3 v4 | last revised 2025.12.04

© BittWare 2025

Agilex is a trademark of Intel Corp. All other products are the trademarks or registered trademarks of their respective holders.

