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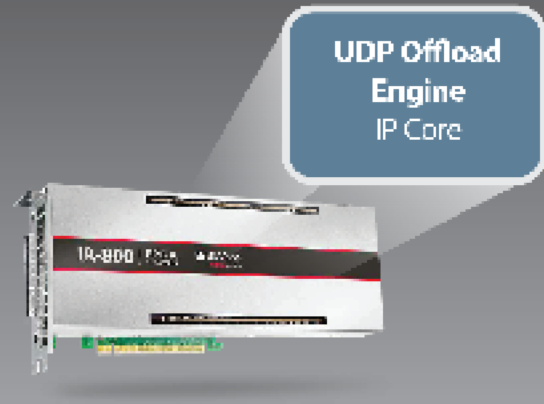
Partner IP Core

Atomic Rules

UDP Offload Engine
IP Core



UOE IP Core for 10/25/50/100GbE

Atomic Rules UDP Offload Engine (UOE) is a UDP FPGA IP Core that allows for immediate operation at 10, 25, 40, 50, or 100GbE. The UOE IP core implements the UDP standard RFC 768, including checksum, segmentation and reassembly hardware offload.

This offloads much of the work described in RFC 768 from software to hardware. In doing so, line rates of 25, 50, and 100GbE are achievable.

The UOE IP core enables application-level UDP datagrams to be concurrently sent and received on a LAN or across a network. An integral IGMPv2 multicast pre-selector removes unwanted traffic, and L4 UDP multicasts are pre-selected so that user applications don't have to perform this function. The UOE IP core is tested for operation with popular FPGA vendors' Ethernet MACs.

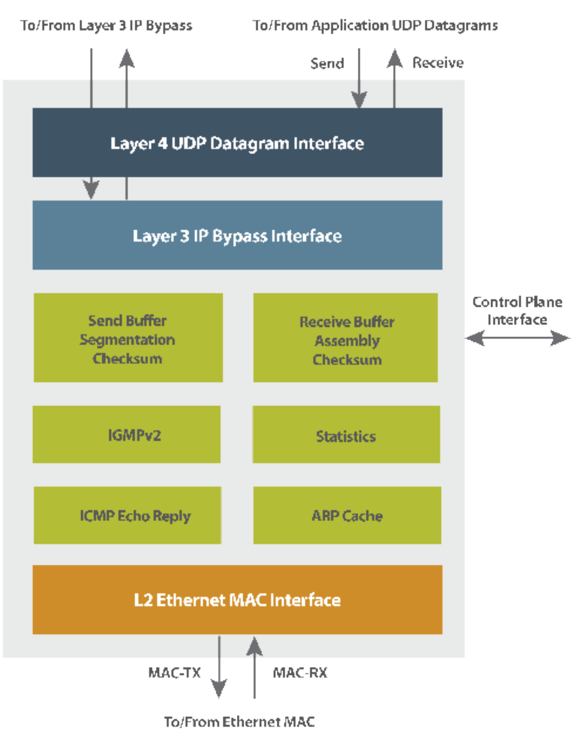
Offload UDP at full line rate up to 100GbE

key features

Full line rate with **no packet loss**

Operate at any line rate up to **100GbE**

Offloads UDP standard RFC 768



Features

- Future proof your application; optimize throughput for all line rates
- Operates at 10/25/50/100GbE
- Run full line rate with no packet loss, even for very small packets
- Offloads UDP standard RFC 768 from software to hardware
- Robust multicast support

UDP Offload Engine

IP Core

Product Operation

RTL sequential circuits in the UOE IP core handle the real-time interconversion of user datagrams and Ethernet frames. The core can function simultaneously as a UDP Sender and a UDP Receiver.

To send a datagram, the core is presented with a datagram and metadata describing the destination and port. If the MAC address for the destination IP address is unknown, the ARP circuit in the core resolves it. If the PDU of the datagram being sent exceeds the MTU, the core segments the datagram into fragments.

To receive, the core listens for Ethernet frames that encapsulate a UDP/IP payload. If the checksums are correct, it forms the datagram out of one or more fragments. When an entire datagram is ready, it is presented to the application logic along with its metadata.

When receiving multicast datagrams, the core preselects and delivers to the application only the host groups that have been joined by IGMP. This capability offloads the task of decoding the 228 ClassD multicast addresses to a 4-bit code encoding 16 host groups.

Detailed Feature List

- UDP/IPv4 (RFC 768, RFC 791)
- Hardware checksum, segmentation, and reassembly offload
- Multicast (IGMPv2) capability
  - Join and leave support for receiving 16 Class-D groups
  - Send and receive multicast host groups
  - Receive pre-selecting offload (discard of unsubscribed multicasts)
- Concurrent datagram send and receive
- Ethernet packet: programmable frame MTU up to 16K Bytes (Super-Jumbo Frame support)
- UDP packet arbitrary datagram PDU up to IPv4 limit of 64K Bytes
- 16 Entry ARP cache (RFC 826)
- ICMP (unsegmented echo response message type only, used by "ping")
- VLAN (IEEE 802.1Q) support
- Layer 3 direct, allowing non-UDP application connectivity
- Statistics accessible by control-plane interface
- Low-Area implementation, allowing multiple core instances per FPGA
- Industry-standard AXI4 Interfaces (Avalon-Adapted on Intel devices)

Reference Examples

Atomic Rules offers UDP IP reference designs for a range of BittWare cards. Atomic Rules UOE IP Core can operate at up to 400 MHz in such cases where 25 GbE must be implemented with the smallest footprint possible.

Deliverables

The IP core is available in Named-Project or Site-License forms. Both versions include the elements needed for implementation, including a self-validating test bench. Most of the verification IP is also synthesizable, enabling testing to be performed at line rate, not just within a Verilog simulator.

Named-Project: Allows the product to be used on one named project from development through production using one or more bitstreams including compiled versions of the product on authorized FPGA device(s). The project SLA prohibits use on derivative projects.

Site-License: Allows the product to be used at one authorized location from development through production using one or more bitstreams including compiled versions of the product on authorized FPGA device(s). The site SLA allows the product's use on derivative projects from the authorized location.

Sample Implementation Results

Core	Device	LUT	Register	BRAM	Fmax
64B	AMD (Xilinx)	78K	74K	59	400MHz
	Intel (Stratix & Agilex)	73K	123K	230 M20K	500MHz (Agilex)
8B	AMD (Xilinx)	22K	21K	44	400MHz
	Intel (Stratix & Agilex)	23K	32K	88 M20K	500MHz (Agilex)

Compatible FPGA Cards

The UOE IP is compatible with all current BittWare cards with Xilinx UltraScale+, Intel Stratix 10 and Intel Agilex FPGAs.

To learn more, visit **www.BittWare.com**

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