

BittWare
a molex company

AV-870p
PCIe Adaptive SoC Card

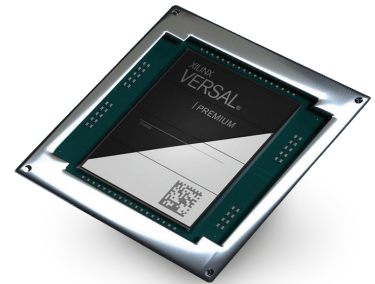


Versal™ Premium Adaptive SoC Card

400G and PCIe Gen5

Brought to market in partnership with LDA Technologies, the AV-870p is a PCIe Gen5 accelerator card designed to deliver extreme performance for data center and edge compute workloads. Featuring the AMD® Versal Premium adaptive SoC, the AV-870p is a deployment-ready full height, ¾ length PCIe accelerator compatible with high-performance servers. The card features QSFP-DDs for up to 4x 400GbE, PCIe Gen5 x8x8, and a sophisticated Board Management Controller (BMC) for advanced system monitoring and control.

AMD

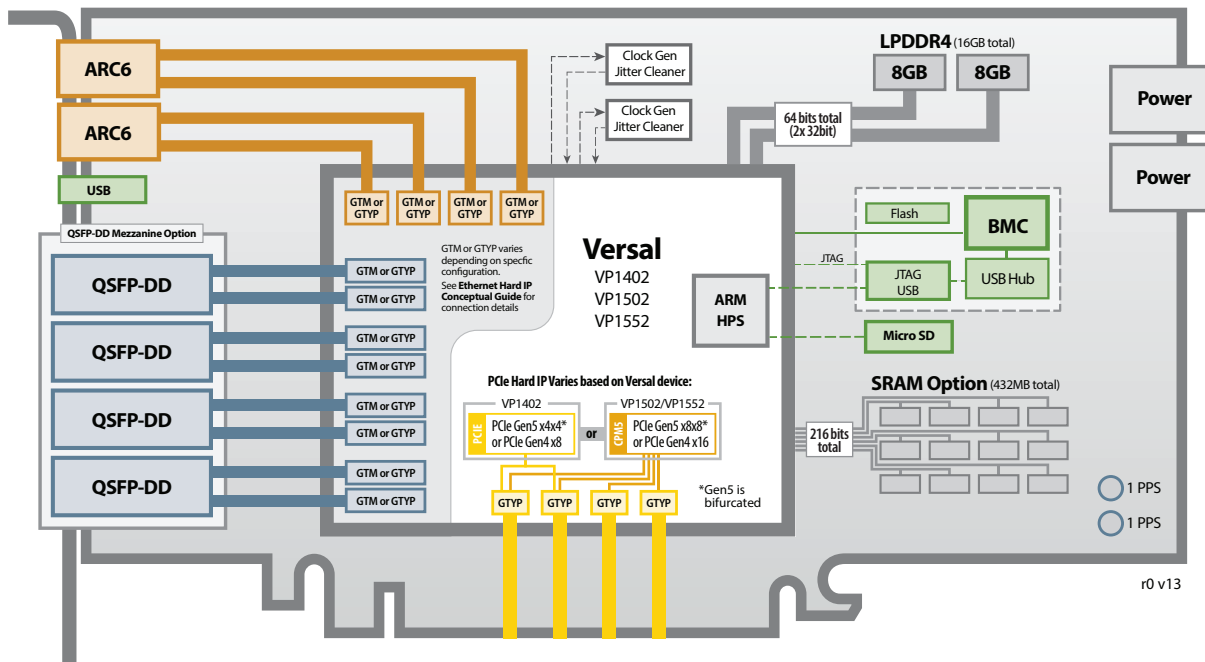


key features

Up to
4x 400GbE

PCIe Gen5
x8x8

Versal Premium
with up to 3.8M
Logic Cells



r0 v13

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Ethernet Hard IP Conceptual Guide

Diagrams below show the basics of Hard IP blocks available for Ethernet. These diagrams are intended only to give a high-level understanding of possible configurations of network ports.

Contact us for specific capability questions at [BittWare.com/contact](https://www.bittware.com/contact).

Transceiver lane speed options for Ethernet

GTM

Each GTM: 4x lanes at 10G NRZ, 25G NRZ or PAM4, or 50G PAM4 (other non-Ethernet rates available)

GTYP

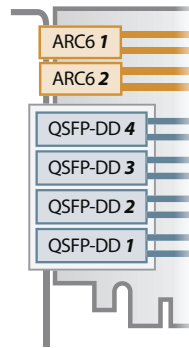
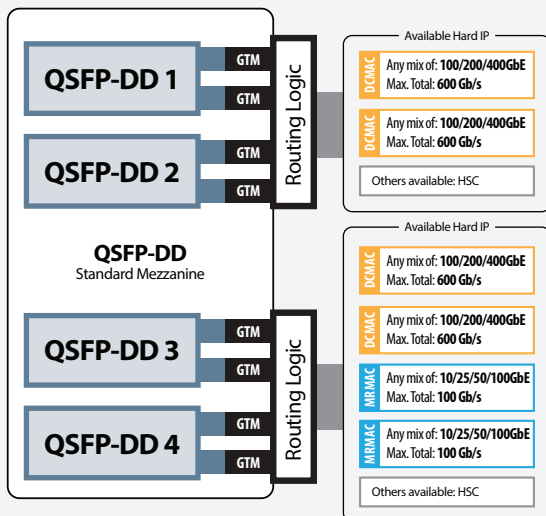
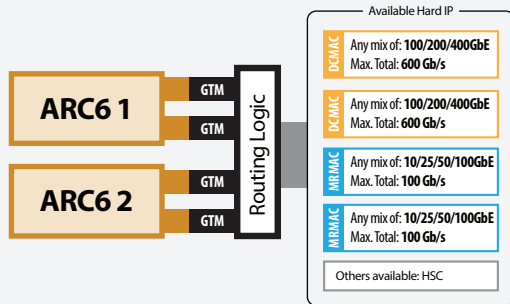
Each GTYP: 4x lanes at 10G or 25G NRZ (other non-Ethernet rates available)

Typical features driving chip/mezzanine options

Your particular needs will drive which is the best combination of chip and mezzanine:

Versal VP1402+ Standard QSFP-DD Mezz.	Maximize 400 GbE Ports (4x) (more using select TeraBox chassis)
Versal VP1502+ Standard QSFP-DD Mezz.	Balance of network ports and chip resources
Versal VP1552+ GTYP QSFP-DD Mezz.	Maximize GTYPs for low-latency and sub-10G (non-Ethernet) rates

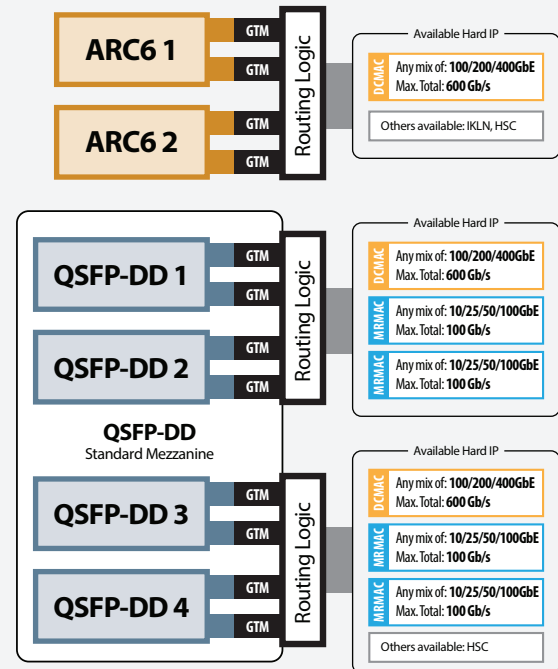
Options using Versal **VP1402** and Standard QSFP-DD Mezzanine



Port Locations Map

For this guide, each ARC6 and QSFP-DD port is numbered as shown. Always defer to the HRG for port addressing from a development standpoint.

Options using Versal **VP1502** and Standard QSFP-DD Mezzanine



Using the dual ARC6 interfaces

One way to utilize the ARC6 connectors is as part of select TeraBox systems with front-panel QSFP-DDs that internally route to the card's transceivers through the ARC6 interfaces.

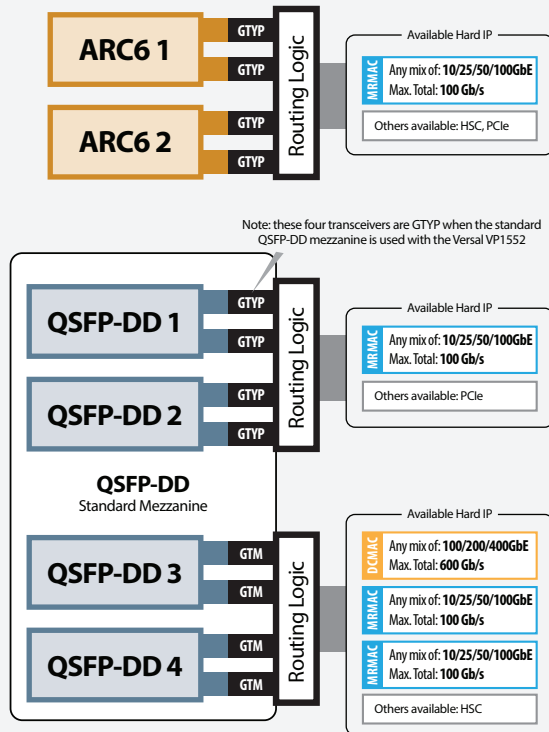
Options for card and server configurations vary. We recommend contacting us for more details at [BittWare.com/contact](https://www.bittware.com/contact).



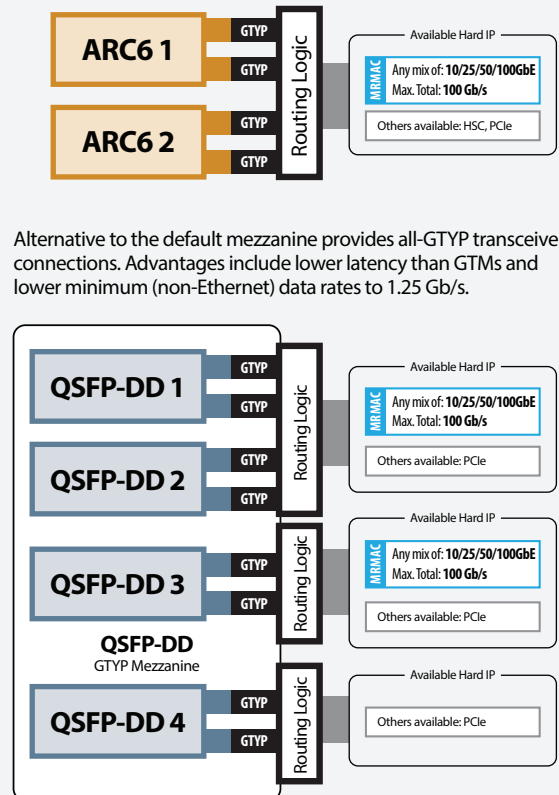
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Options using Versal VP1552 and Standard QSFP-DD Mezzanine



Options using Versal VP1552 and GTYP QSFP-DD Mezzanine



Example uses for specific Ethernet rates

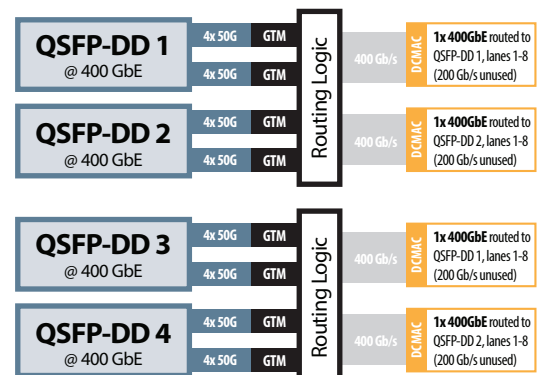
Below are examples of how specific desired Ethernet rates can be achieved. **Many more configurations are possible** based on chip features, mezzanine options, user routing logic, and transceiver configuration. Specific Ethernet modules/cables required will also vary based on configuration, and often require breakout cables.

EXAMPLE 1

4x 400 GbE

This first example pairs the Versal 1402 with the standard QSFP-DD mezzanine for 4x 400 GbE ports in a dual-slot configuration.

Need more 400 GbE ports? Talk to us about utilizing the ARC6 interfaces plus an additional pair of GTMs within TeraBox server chassis options at BittWare.com/contact.



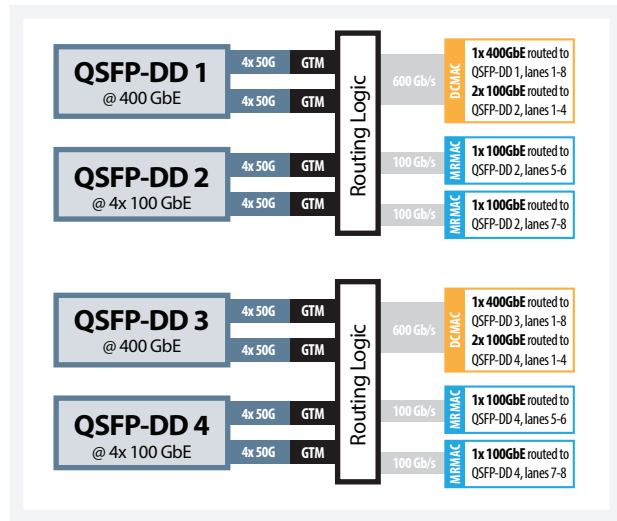
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EXAMPLE 2

2x 400 GbE + 8x 100 GbE

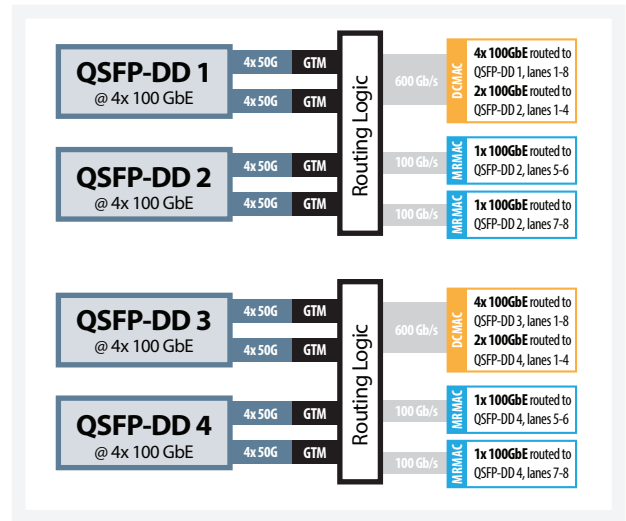
Maximizing 400G and 100G bandwidth using the standard QSFP-DD mezzanine and the VP1502 device.



EXAMPLE 3

16x 100 GbE

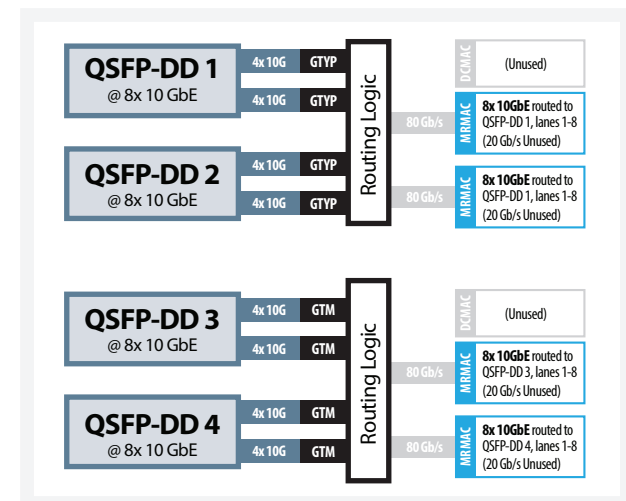
This example is very similar to #2, except we've exchanged two 400 GbE links for eight 100 GbE for a total of 16x 100 GbE on the VP1502.



EXAMPLE 4

32x 10 GbE

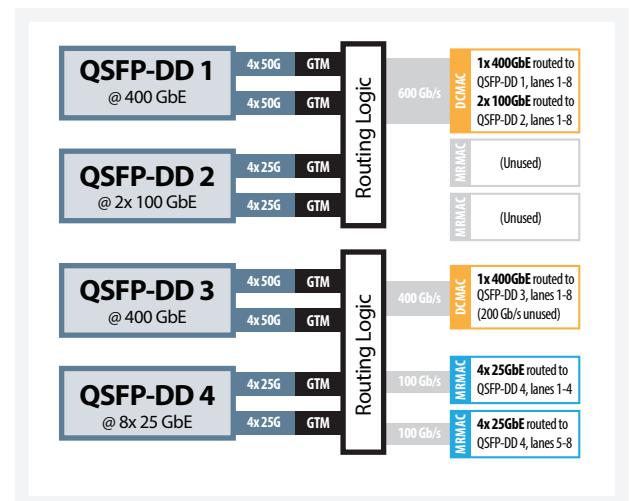
This example uses the standard QSFP-DD mezzanine and the Versal VP1552 device.



EXAMPLE 5

2x 400 GbE + 2x 100 GbE + 8x 25 GbE

This example uses the standard QSFP-DD mezzanine and the Versal VP1502 device.



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Board Specifications

Adaptive SoC	- Versal Premium - VP1402/VP1502/VP1552 - Core speed grade - 2 - Contact BittWare for other FPGA options
On-board Flash	Flash memory for booting FPGA
External memory	2x 8GB LPDDR4 chips (16GB total) @ 4266MHz (64 bits) accessible to ARM and FPGA logic via NOC 432 MB of ultra-low-latency GSI SRAMs (optional) 12x 18-bit chips 216-bit total bus width
Host interface	- PCIe Gen5 x8x8 (bifurcated) or PCIe Gen4 x16 connected to PCIe w/DMA (CPM5) Hard IP (VP1502/VP1552) - PCIe Gen5 x4x4 (bifurcated) or PCIe Gen4 x8 connected to PCI Express Hard IP (VP1402)
I/O Expansion	- I/O expansion site connected to FPGA via 48x SerDes channels 2x ARC6-16 connectors connected to FPGA via 8x SerDes channels each (16x total)
QSFP-DD Module	- Default I/O module features 4x QSFP-DD cages - Additional modules available (contact BittWare)
Clocking	2x Jitter cleaners for network recovered clocking 2x 1PPS (in-board)
USB	USB access to BMC, USB-JTAG, USB-UART

Board Management Controller	- Onboard CLI - Python, C++ API (contact BittWare) 200 Mbps parallel port connected to the FPGA fabric and the NOC - USB SD Card Reader for simple OS images transfer to ARM processors - Fast FPGA boot flash programming - Temperature, voltage, current monitoring - SNMP agent for centralized management - Dedicated preprogrammed array of 32 MAC addresses - I/O port monitoring full QSFP, SFP, QSFP-DD access and programming through CLI and API - CLI-based clock selection supporting custom clock configurations
Cooling	Standard: dual-width passive heatsink
Electrical	- On-board power derived from 12V PCIe slot and 2x AUX connectors - Power dissipation is application dependent
Environmental	Operating temperature 5°C to 35°C
Form factor	¾-length, standard-height PCIe dual-width board 10 x 4.37 inches (254 x 111.15 mm)

Development Tools

Application development	Supported design flows -Vivado Design Suite (HDL, Verilog, VHDL, etc.)
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Safety & Compliance

- FCC (USA) 47CFR15.107 / 47CFR15.109
- CE (Europe) EN55032:2015 + A11:2020 / EN55035:2017 + A11:2020 / EN61000-3-2:2019 +
- UKCA (United Kingdom) BS EN55032:2015 + A11:2020 / BS EN55035:2017 + A11:2020 / BS
- ICES (Canada) ICES-003 Issue 7 October 2020
- RoHS compliant to the 2011/65/EU + 2015/863 directive



Embedded
Partner
Program

PREMIER

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