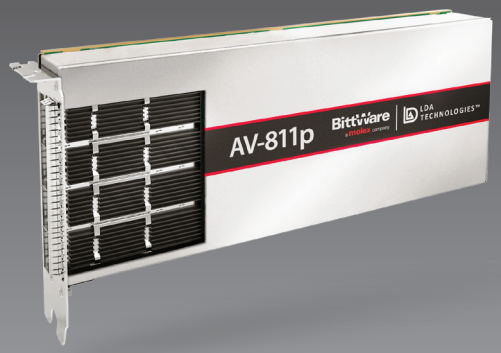
BittWare a molex company

AV-811p

PCIe Adaptive SoC Card



LDA

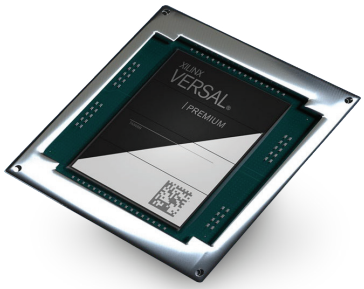
Preliminary Product Info

This document is preliminary for a product that has not been announced. It is not for public release or distribution.

Versal™ Premium Adaptive SoC Card

AI Engine* and 2x the logic and memory of other Versal adaptive SoCs

AMD

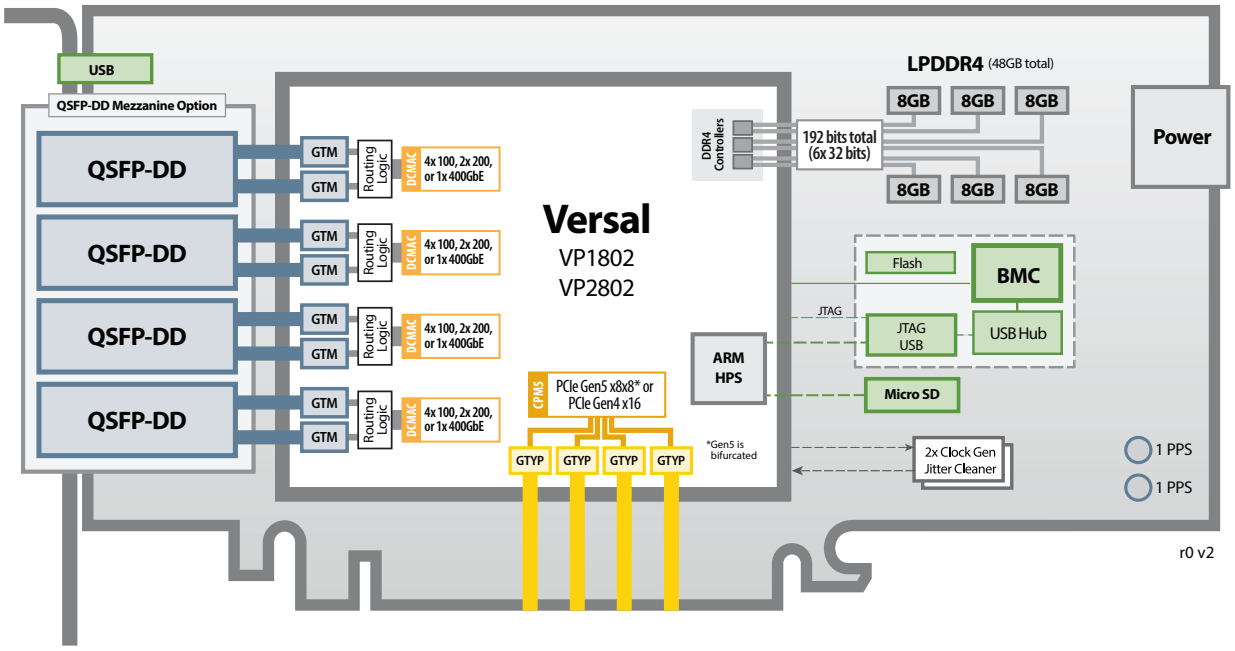


Brought to market in partnership with LDA Technologies, the AV-811p is a PCIe Gen5 accelerator card designed to deliver extreme performance for data center and edge compute workloads. Featuring AMD Xilinx®'s Versal Premium adaptive SoC, the AV-811p is a deployment-ready full height, ¾ length PCIe accelerator compatible with high-performance servers. The card features QSFP-DDs for up to 4x 400GbE, LPDDR4 memory, PCIe Gen5 x8x8, AI engine,* and a sophisticated Board Management Controller (BMC) for advanced system monitoring and control.

** Available on VP2802 only.*

key features

- Up to **4x 400GbE**
- **PCIe Gen5** x8x8
- **Versal Premium** **7.3M** System Logic Cells **14.3K** DSP Engines

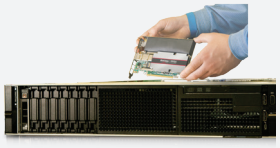


Additional Services

Take advantage of BittWare's range of design, integration, and support options

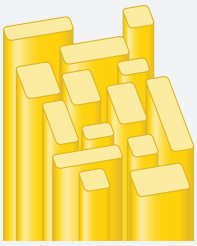
Customization

Additional specification options or accessory boards to meet your exact needs.



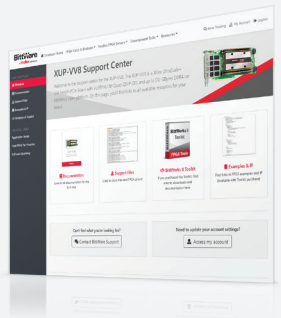
Server Integration

Available pre-integrated in our TeraBox servers in a range of configurations.



IP and Solutions

Our portfolio of IP and solutions reduce risk for development and deployment.



Service and Support

BittWare Developer Site provides online documentation and issue tracking.

Board Specifications

Adaptive SoC	• Versal Premium
	  • VP1802 or VP2802
	  • Core speed grade - 2
	• AI engines (VP2802)
	  • 472 AI Engine Tiles
	  • 118Mb AI Engine Memory
	• Contact BittWare for other FPGA options

On-board Flash	• Flash memory for booting FPGA
External memory	• 48GB LPDDR4
Host interface	• PCIe Gen5 x8x8 (biifurcated) interface direct to FPGA, connected to PCIe Hard IP
QSFP-DD Module	• Optional QSFP-DD I/O module with 4x QSFP-DD cages connected to FPGA via 8x SerDes channels each (32x total)
Clocking	• 2x Jitter cleaners for network recovered clocking • 2x 1PPS (in-board)
USB	• USB access to BMC, USB-JTAG, USB-UART
Board Management Controller	• Onboard CLI • Python, C++ API (contact BittWare) • 200 Mbps parallel port connected to the FPGA fabric and the NO • USB SD Card Reader for simple OS images transfer to ARM processors • Fast FPGA Boot Flash programming • Temperature, voltage, current monitoring • SNMP agent for centralized management • Dedicated preprogrammed array of 32 MAC addresses • I/O port monitoring full QSFP, SFP, QSFP-DD access and programming through CLI and API • CLI-based clock selection supporting custom clock configurations
Cooling	• Standard: dual-width passive heatsink
Electrical	• On-board power derived from 12V PCIe slot and 12-pin AUX connector • Power dissipation is application dependent
Environmental	• Operating temperature 5°C to 35°C
Form factor	• ¾-length, standard-height PCIe dual-width board • 10 x 4.37 inches (254 x 111.15 mm)

Development Tools

Application development	Supported design flows -Vivado Design Suite (HDL, Verilog, VHDL, etc.)

AMD Embedded Partner Program PREMIER

To learn more, visit **www.BittWare.com**

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LDA TECHNOLOGIES™

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