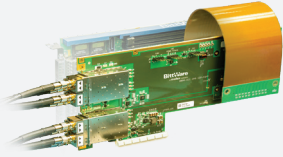




# Additional Services

Take advantage of BittWare's range of design, integration, and support options



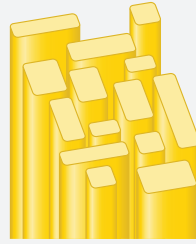
## Customization

[Additional specification options](#) or [accessory boards](#) to meet your exact needs.



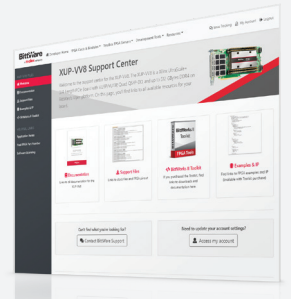
## Server Integration

Available pre-integrated in our [TeraBox servers](#) in a range of configurations.



## Application Optimization

Ask about our services to help you port, optimize, and benchmark your application.



## Service and Support

BittWare Developer Site provides online documentation and issue tracking.

## Board Specifications

FPGA	<ul style="list-style-type: none"> <li>Intel Stratix 10 NX                             <ul style="list-style-type: none"> <li>NX2100 in an F2597 package</li> <li>8GBytes on-chip High Bandwidth Memory (HBM2) DRAM, 410 GB/s (speed grade 2)</li> <li>Core speed grade -2: I/O speed grade -2</li> </ul> </li> <li>Contact BittWare for other Stratix 10 NX options</li> </ul>
On-board Flash	<ul style="list-style-type: none"> <li>2Gbit Flash memory for booting FPGA</li> </ul>
External memory	<ul style="list-style-type: none"> <li>2x 288-pin DIMM slots each fitted with 16GB modules by default, i.e., 32GB total on board (options up to 256GB total)</li> <li>Contact BittWare for QDR-II+ DIMM options</li> </ul>
Host interface	<ul style="list-style-type: none"> <li>x16 Gen3 interface direct to FPGA, connected to PCIe hard IP</li> </ul>
QSFP cages	<ul style="list-style-type: none"> <li>4 QSFP28 cages on front panel connected directly to FPGA via 16 transceivers</li> <li>User programmable low jitter clocking supporting 10/25/40/100GbE</li> <li>Each QSFP28 can be independently clocked</li> <li>Jitter cleaner for network recovered clocking</li> <li>2 QSFP28s have available 100GbE MAC hard IP</li> </ul>
OCuLink	<ul style="list-style-type: none"> <li>2x edge connectors (A, B) @ 12.5G per lane (default); each supports PCIe Gen 3 x8 hard IP, GPIO, and PCIe master and optional input clocking</li> <li>2x inner connectors (C, D) @ 25G per lane (optional); 1x 100GbE MAC hard IP per OCuLink</li> </ul>
Board Management Controller	<ul style="list-style-type: none"> <li>Voltage, current, temperature monitoring</li> <li>Power sequencing and reset</li> <li>Field upgrades</li> <li>FPGA configuration and control</li> <li>Clock configuration</li> <li>Low bandwidth BMC-FPGA comms with SPI link</li> <li>USB 2.0</li> <li>PLDM support</li> <li>Voltage overrides</li> </ul>

Cooling	<ul style="list-style-type: none"> <li>Standard: double-width active heatsink (with fan)</li> <li>Optional: double-width passive heatsink</li> <li>Optional: double-width liquid cooling</li> </ul>
Electrical	<ul style="list-style-type: none"> <li>On-board power derived from 12V PCIe slot &amp; two AUX connectors (one 8-pin, one 6-pin)</li> <li>Power dissipation is application dependent</li> <li>Typical max power consumption 225W</li> </ul>
Environmental	<ul style="list-style-type: none"> <li>Operating temperature: 5°C to 35°C</li> </ul>
Quality	<ul style="list-style-type: none"> <li>Manufactured to IPC-A-610 Class 2</li> <li>RoHS compliant</li> <li>CE, FCC, UKCA &amp; ICES approvals</li> </ul>
Form factor	<ul style="list-style-type: none"> <li>Standard-height PCIe dual-slot board</li> <li>111.15mm x 266.70mm (4.376in x 10.500in)</li> </ul>

## Development Tools

FPGA development	BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateway, PCIe driver & host test application)
Application development	Supported design flows - Quartus Prime Pro (HDL, Verilog, VHDL, etc.)

## Deliverables

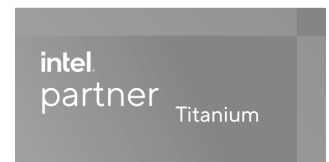
- 520NX FPGA board
- USB cable (front panel access)
- Built-In Self-Test (BIST)
- 1-year access to online Developer Site
- 1-year hardware warranty

To learn more, visit [www.BittWare.com](http://www.BittWare.com)

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