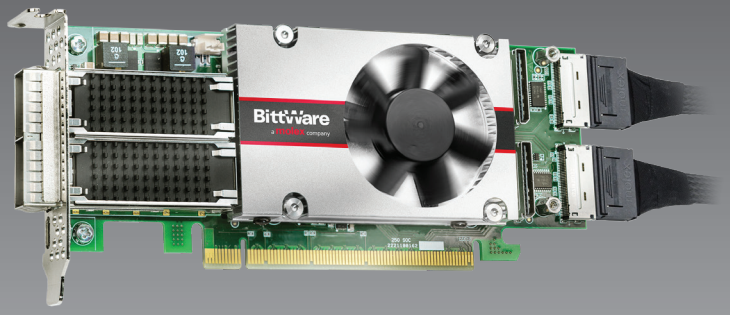
BittWare a molex company

# 250-SoC

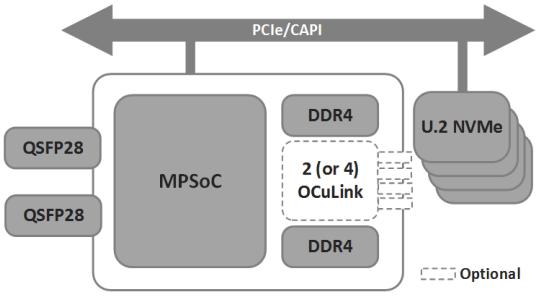
DAA and NVMe-oF




## Directly Attached Accelerator & NVMe-over-Fabric

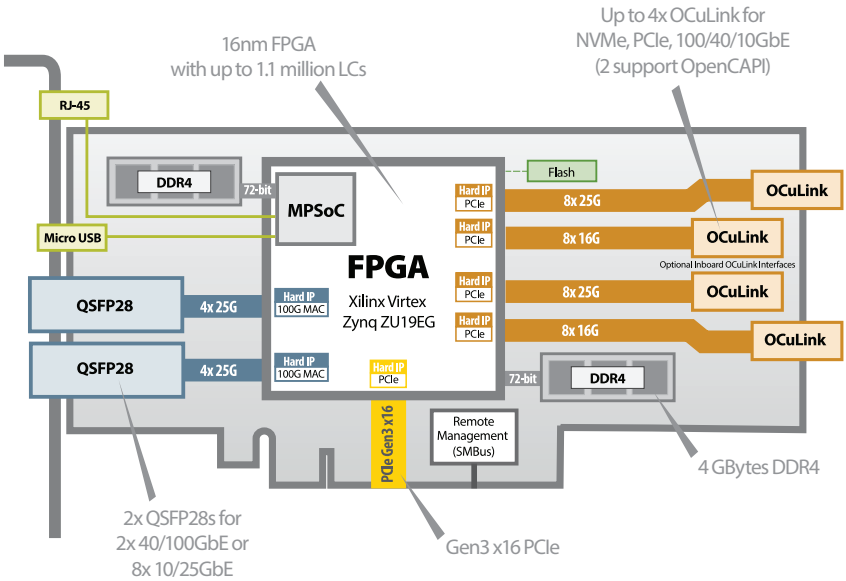
**Reliable transport of NVMe frames with low latency and high throughput**

The 250-SoC enables the creation of remote, disaggregated storage or Ethernet Just-a-Bunch-of-Flash (EJBOF) to dramatically reduce the storage cost, footprint and power within data centers. The 250-SoC features a Xilinx Zynq UltraScale+ MPSoC device featuring both programmable logic and 64-bit ARM processors. This powerful, feature-rich device coordinates data transfer between two 100GbE network ports, on-board DDR4 memory and a PCIe Gen 3 host interface.




## key features

- **2x 100GbE** via 2 QSFP28
- Ideal for **NVMe** storage arrays
- ZU19EG MPSoC: **64-bit Cortex A53 ARM** Zynq UltraScale+




### Accelerating High Level Design

- Vivado HLx Editions supply design teams with the tools and methodology needed to leverage C-based design and optimized reuse
- Includes IP sub-system reuse, integration automation and accelerated design closure
- When coupled with the UltraFast™ High-Level Productivity Design Methodology Guide, this unique combination is proven to accelerate productivity
- It enables designers to work at a high level of abstraction while facilitating design reuse

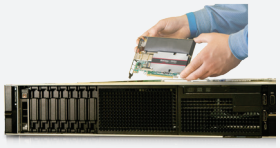
VIVADO HL*x* Editions

# Additional Services

Take advantage of BittWare's range of design, integration, and support options

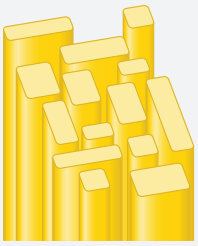
## Customization

Additional specification options or accessory boards to meet your exact needs.



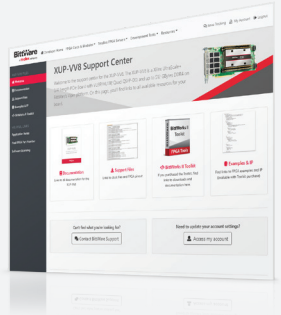
## Server Integration

Available pre-integrated in our TeraBox servers in a range of configurations.



## IP and Solutions

Our portfolio of IP and solutions reduce risk for development and deployment.




## Service and Support

BittWare Developer Site provides online documentation and issue tracking.

## Specifications

| | |
|---|---|
| **FPGA** | • Xilinx Zynq UltraScale+<br>  • ZU19EG FFVD1760 package<br>  • Core speed grade -2<br>  • Application ARM: Quad-core Cortex-A53 MP-Core 1.5GHz<br>  • Real-Time ARM: Dual-core Cortex-R5 MPCore 600MHz<br>  • Graphics Processor: Mali-400 MP2<br>• Contact BittWare for other MPSoC options |
| **On-board DDR4 SDRAM** | • DDR4 SDRAM FPGA Fabric Memory<br>  • One 4GB bank of DDR4 SDRAM x72 bits<br>  • Transfer Rate: 2400 MT/s<br>• DDR4 SDRAM MPSoC Memory<br>  • One 4GB bank of DDR4 SDRAM x72 bits<br>  • Transfer rate: 2400 MT/s |
| **Host interface** | • x16 mechanical PCIe Gen3 capable<br>• Configurable as x16 up to Gen3, or two x8 PCI in bifurcated slots |
| **QSFP cages** | • 2 front panel 4-25Gbps-lane QSFP28 cages<br>• User programmable low jitter clocking supporting 10/25/40/100GbE<br>• Each QSFP28 can be independently clocked |
| **OCuLink** | • 1 back panel 8-25Gbps-lane OCuLink connector<br>• 1 back panel 8-16Gbps-lane OCuLink connector<br>• Flexible configuration: NVMe, PCIe, 10/40/100GbE, OpenCAPI<br>• 2 additional optional 8-lane OCuLink connectors (25 & 16Gbps) |
| **Board control (front panel)** | • RJ45 1GbE access to the ARM processor<br>• USB connector for UART to ARM processor |
| **Datacenter Deployment, Health Monitoring & Reporting** | • On-board power, voltage and temperature monitoring<br>• Field flash update via software<br>• SMBus controlled anti-bricking, fallback and multi-boot<br>• SMBus access to unique board data and temperature sensor |
| **Cooling** | • Active and passive heatsink options |
| **Electrical** | • On-card power derived from PCIe slot supplies<br>• Power dissipation is application dependent<br>• Typical FPGA power consumption ~50W |
| **Environmental** | • Operating temperature: 5°C to 35°C |
| **Quality** | • Manufactured to IPC-A-610 Class 2<br>• RoHS compliant |
| **Form factor** | • Half-height, half-length PCIe board<br>• Full-height PCI bracket option<br>• 68.90mm x 167.65mm (2.713in x 6.600in) |

## Development Tools

| | |
|---|---|
| **FPGA development** | BIST - Built-In Self-Test for CentOS 7 provided with source code (pinout, gateware, PCIe driver and host test application) |
| **Application development** | Xilinx Tools - Vivado Design Suite HLx Editions: HDL and C/C++ with HLS |

## Deliverables

- 250-SoC FPGA board
- Built-In Self-Test (BIST)
- 1-year access to online Developer Site
- 1-year hardware warranty

To learn more, visit **www.BittWare.com**

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