IMPLEMENTING HARDWARE ACCELERATION IN FINANCIAL MARKETS

A step change in speed
IF YOU COULD VALUE YOUR PORTFOLIO FASTER, WOULD IT HELP YOUR BUSINESS?
How about if you could value it 1,000 times faster?

For many years, PA Consulting Group has had a strong capability in building and implementing hardware acceleration solutions in the mobile telecommunications sector.

We have helped mobile communication devices to deliver ever-increasing data bandwidths by using parallel architectures in hardware to speed-up signal-processing algorithms, which have traditionally been carried out in sequential software architectures.

We are now joining this proven hardware acceleration capability, with our capital markets sector experience to demonstrate what might be possible for financial firms.

Valuing the global portfolios of large financial firms is very resource intensive. It often involves discounting several hundred million cash flows to present value and has historically taken up to 5-hours to complete. PA has taken this specific challenge and using a Field Programmable Gate Array (FPGA) platform, we have shown that it is possible to give companies almost real time portfolio valuation information.

PA has implemented a portfolio valuation process on an Field Programmable Gate Array (FPGA) platform and reduced the time for processing a portfolio of 50 million cash flows from several hours to under 1 second.

Rapid portfolio valuation can allow firms to make more money by trading confidently at times of high volatility or it can allow firms to release risk capital for better business use. This can be achieved through working with PA.
The processes used to calculate the value and risk exposure of the portfolio are extremely repetitive and amount to tens or hundreds of millions of sequential operations, often using a sub-optimum software platform, resulting in hours of running time to generate the solution.

The very nature of the problem in software presents the ideal scenario for optimum results using a Field Programmable Gate Array (FPGA): i.e., the repetitive nature of the processing means it is ideal for running in a highly parallel architecture, reducing the elapsed time by handling many tasks simultaneously.

FPGAs are electronic devices offering a ‘sea-of-gates’ that can be configured to perform any digital processes independently.
Repetition, repetition, repetition

We have taken a typical approach to determining the trade portfolio Net Present Value (NPV) and designed this into a form suitable for parallel processing on a Field Programmable Gate Array (FPGA). Figure 1 illustrates the top-level architecture.

PA’s system implementation for benchmarking this acceleration:

- Takes a portfolio of GBP denominated Gilt futures contracts
- Establishes a GBP zero coupon yield curve to discount the future cash flows
- Discounts the future cash flows to present value, summing the results to provide a portfolio valuation
- Handles a single currency (this can be scaled to more parallelism for no extra latency introduction)
- Assumes coupon rates and market prices will always be available at 6 monthly intervals on 7 March and 7 September every year
- Handles the date range 1st January 2000 to 31st December 2127
- Uses coupon rates at multiples of 0.25%
- Takes market prices in multiples of 0.005
- Calculates zero coupon rates at 6 monthly intervals
- Uses cubic spline interpolation between the 6 monthly zero coupon rates to obtain daily zero coupon rates
We implemented the system on an Altera Stratix V FPGA running on a BittWare SSPE card suitable for financial use.

We have verified our calculations against spreadsheet results, giving high confidence in the approach we have adopted.

- **At a clock frequency of 100MHz, the system handles a portfolio of 50 million cash flows in 0.5 of a second.** This equates to one cash flow processed for each clock cycle. By doubling the clock frequency the stated processing time could be halved.

- **There is plenty of scope for more intensive use on the same chip.** Our FPGA implementation uses around 15% of its resources meaning extra scenarios can be calculated in parallel in the same time period. The portfolio can be significantly extended in scale on the same chip. Alternatively, multi-currency processing and risk scenarios of the yield curve could be added.

- **There is no degradation in processing speed with increased scale.** The system is easily scalable by adding more chips or cards.

- **The system is highly deterministic,** which reduces the risk of error through higher test coverage. Further, latency will not vary under different operating conditions as can be experienced in software systems.

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We have developed and implemented a hardware acceleration solution for portfolio valuation. We have achieved a 1,000 times improvement in the latency compared with implementations using typical non-optimised software platforms. At such fast rates of calculation, firms would be able to confidently trade during periods of high volatility. At such fast rates of calculation, firms could run risk scenarios against global portfolios rapidly. For example, scenarios could vary interest rates of the zero coupon yield curve before valuation. These scenarios will help to refine the risk capital held against a portfolio leading to reduced capital allocation and cost savings.

PA is happy to share more information on this benchmarking result and help you to incorporate innovative technology solutions in your systems.

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We are an employee-owned firm of over 2,500 people, operating globally from offices across North America, Europe, the Nordics, the Gulf and Asia Pacific.

We are experts in energy, financial services, life sciences and healthcare, manufacturing, government and public services, defence and security, telecommunications, transport and logistics.

Our deep industry knowledge together with skills in management consulting, technology and innovation allows us to challenge conventional thinking and deliver exceptional results with lasting impact.